Platforms for Integrated Photonic Switching Modules

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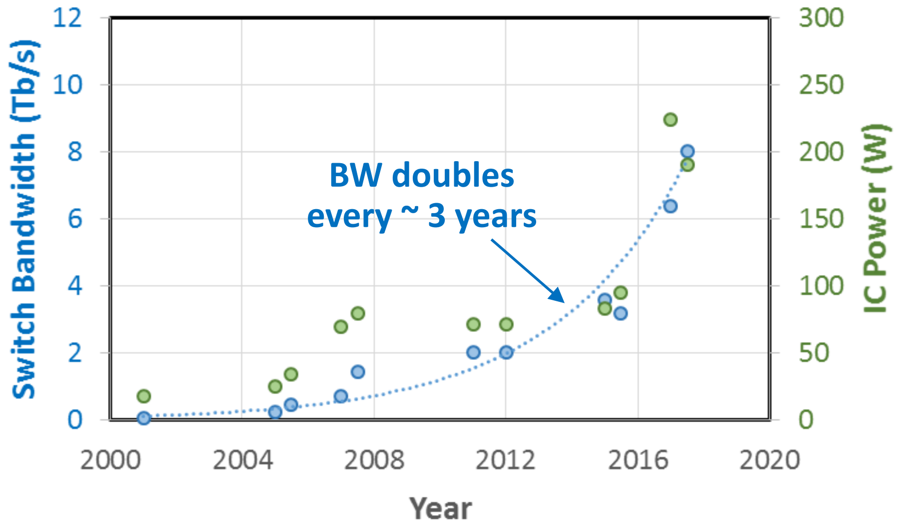
OFC 2019 Workshop: Opportunities and Challenges for Optical Switching in the Data Center

03 March 2019

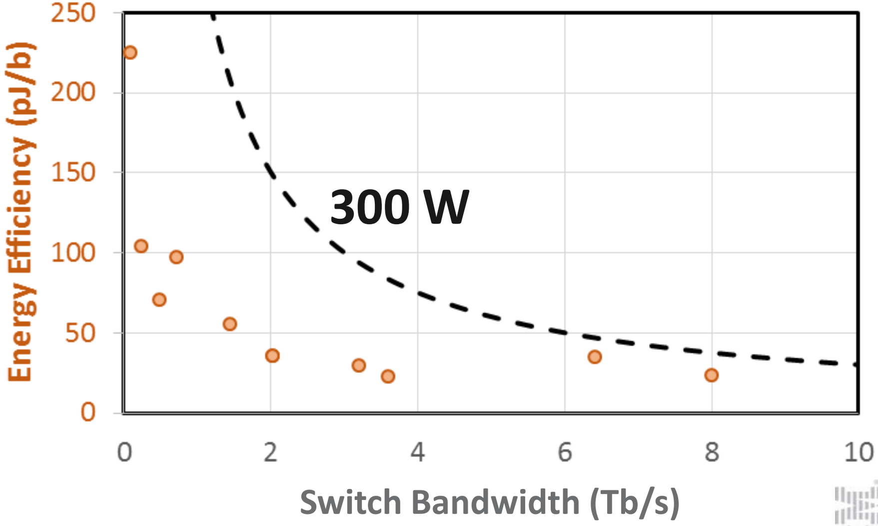
Electrical Packet Switching ASICs Running Into Thermal Power Limits

Published switch IC bandwidth and power performance from a leading switch provider over the past 15+ years



A major technology breakthrough will be needed to allow continued scaling of network bandwidth with reasonable power.

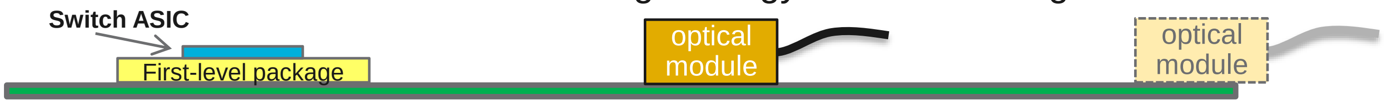
- Power consumption increases with bandwidth
- Power is nearing thermal limits for practical IC cooling
- Efficiency gains from CMOS scaling are beginning to be depleted



The Promise of Optical Switching

Now

On Board Optics



- Bandwidth limited by pin density at package / board interface
- Large energy costs for driving > 10 cm transmission lines

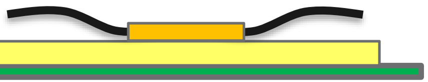
Soon

Co-Packaged Optics

- Bandwidth limited by pin density at chip / package interface
- Some energy required for few cm long transmission lines but dominated by E/O and O/E

Future

Optical Switch



- Bandwidth limited by spectral efficiency – not pin counts
- No E/O or O/E. Energy spent on steering pipes rather than processing or transmitting bits

- **Avoids distortion, power, & cost of ASIC-interfacing electrical links**
- **Moves beyond chip & module pin-count limits**
- **Oblivious to upgrades in signaling rates and formats**

Reconfigurability of Optical Switching Technologies

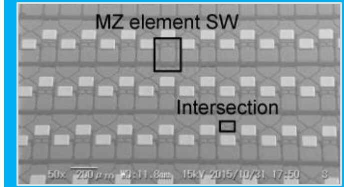
Hybrid circuit/packet networks — Quasi-packet switched networks

Job-level reconfiguration — Flow-level reconfiguration — Packet-level reconfiguration

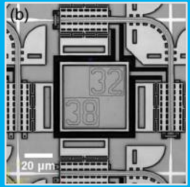
Software control (SDN) — Hardware control (FPGA/ASIC)

s — ms — μs — ns — ps

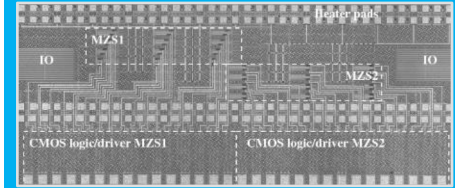
- Fewer ports, Higher loss
- Challenging coupling, crosstalk, & polarization



Thermo-Optic
[OECC 2016, PD2-3]



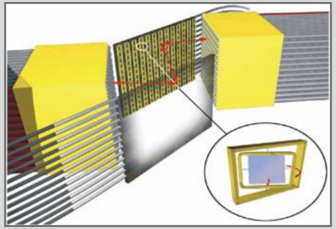
Photonic MEMS
[Optica 2016, **3** (1)]



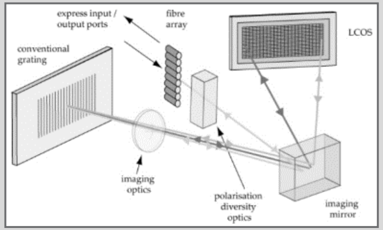
Electro-Optic
[JLT 2015, **33** (20)]

Photonic Switches (Research)

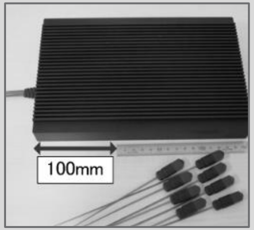
Free-space & Silica-based Switches (Commercial)



3D-MEMS
[J. Opt. Netw. 2007, **6** (1)]



Liquid Crystal
[OFC 2006, OTuF2]



Silica PLC
[Sohma, ECOC 2006]

- 10s - 100s of ports
- Few dBs of insertion loss
- Broadband
- High extinction
- Polarization insensitive

But, photonics promise high density, low power, fast switching, and potentially much lower cost.

State of the Art Photonic Switch Fabrics

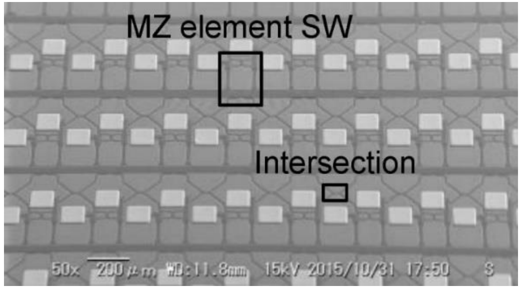
Thermo-optic (TO) switches are the most commercially ready photonic switch technology.

TABLE III
EXEMPLARY SWITCH FABRIC DEMONSTRATIONS

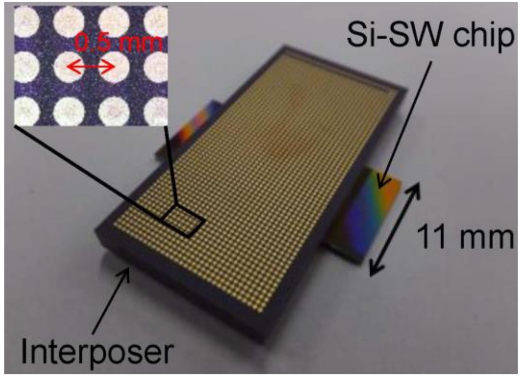
	AIST [77]	Berkeley [50]	IBM [83]
Inputs × Outputs	32×32	64×64	4×4
Cell Architecture	TO MZ	MEMS	EO MZ
Fabric Topology	PILOSS	CSM †	DLN †
Driver Integration	On Card	None	Monolithic
Typical Switching Voltage	2.7 V	18 V	1 V
Chip Package	Ceramic	Ceramic	Wirebond
Module Package	LGA	Wirebond	Not needed
Optical Coupling	Inv. Taper	Grating	Inv. Taper
Optical Package	PLC	PROFA	None
Coup. Loss (dB)	6.8	7.5	-
Chip Loss (dB)	6.4	3.7	3.0
Single-Path Crosstalk (dB)	−19	−60 ‡	−25
Power (W)	1.9	-	0.15
Transient (μs)	30	0.9	0.004

†CSM: crosspoint switch matrix, DLN: double layer network.
‡Extrapolated from measurements on a characteristic elementary cell.

[Lee and Dupuis, *J. Lightw. Technol.* 2019, 37 (1) 6-20]



Mach Zehnder based photonic switch matrix



flip-chip assembled to interposer

packaged system demo

[Suzuki, JLT 2019, vol. 37, no. 1, pp. 116]

State of the Art Photonic Switch Fabrics

MEMS switches have been the most scalable photonic switch technology.

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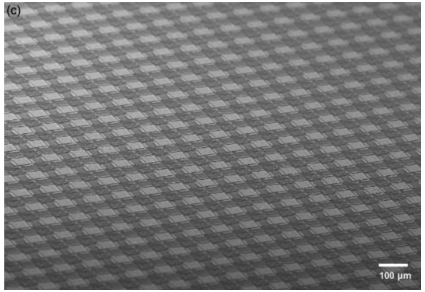
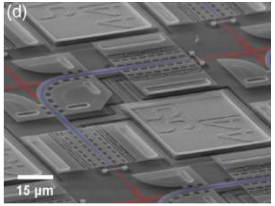
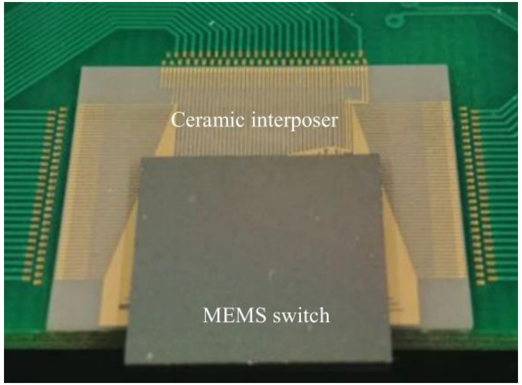
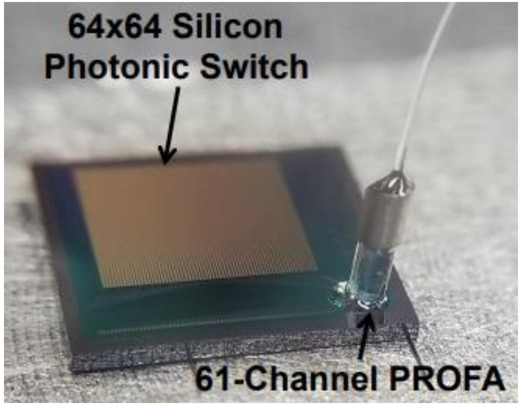




flip-chip demo



multi-fiber coupling demo



[Seok, OFC 2017, Th5D.7]
[Seok, *Optica* 2016, **3** (1) 64]
[Hwang, *Phot J* 2017, **9** (3) 64]

State of the Art Photonic Switch Fabrics

Electro-optic (EO) switches provide the fastest photonic switch reconfigurability.

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[Lee and Dupuis, *J. Lightw. Technol.* 2019, 37 (1) 6-20]

Electro-optic (EO) Switch Fabrics

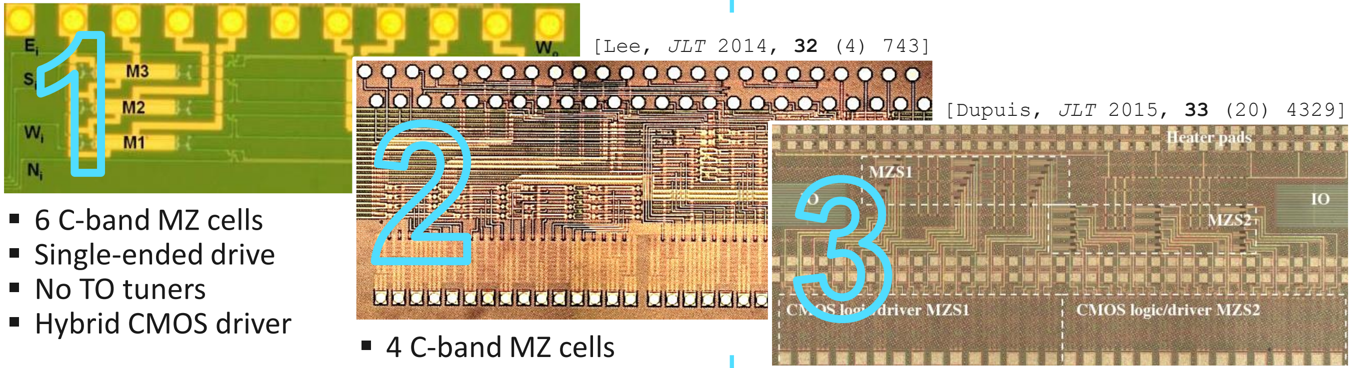
- Based on carrier-injection PIN diode phase shifters
- Reconfigurable at the nanosecond scale
- Must deal with free-carrier absorption (FCA)
- FCA-induced loss and crosstalk limit scale
- More sophisticated cell architectures can overcome FCA
  - Push-pull drive → [N. Dupuis, JLT 2015]
  - Nested cells → [N. Dupuis, OL 2016]
  - Other novel architectures possible
- Higher cell complexity creates packaging challenges
- Benefits greatly from monolithic integration of electronics
- ***New results incorporating novel cell architectures and major advancements in monolithic component integration are pending publication***

3 Generations of IBM 4×4 EO MZ Photonic Switch Systems-on-Chip

[Yang, *Opt. Exp.* 2011, **19** (1) 47]

[Lee, *JLT* 2014, **32** (4) 743]

[Dupuis, *JLT* 2015, **33** (20) 4329]



- 6 C-band MZ cells
- Single-ended drive
- No TO tuners
- Hybrid CMOS driver

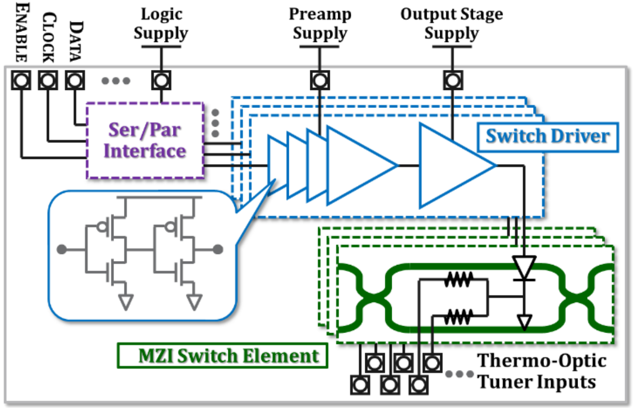
- 4 C-band MZ cells
- Single-ended drive
- TO tuners
- Monolithic CMOS driver

- 12 O-band MZ cells in 3 stages
- Push-pull drive & TO tuners
- Monolithic driver in GF 9WG

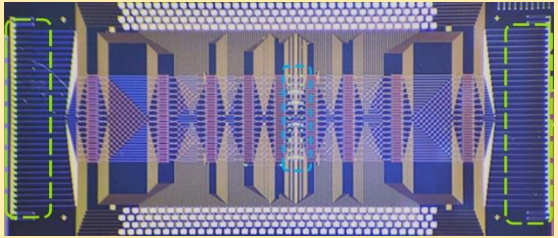
3rd Gen Results

- On-chip loss: 3 dB
- *No optical packaging*
- Crosstalk (single aggressor): < -25 dB for all paths
- Bandwidth: 15 nm
- Switching time: 4 ns
- Power: 150 mW
- Footprint: 15 mm²

monolithic driver integration



Chinese Academy of Sciences, Beijing



[Qiao, *Nature Sci. Rep.* 2017, **7** 42306]

32 × 32	Benes architecture
144	switch cells
0.54 W	power (no heaters)
62.9 mm²	footprint
1.2 ns	switching time
10 dB	F/F coupling loss
18.5 dB	on-chip loss
-15 dB	crosstalk

A Few Words About Ring Resonator Based Switch Fabrics

Ring resonator based switches have potential for area- and power-efficiency advantages.

TABLE IV
THERMO-OPTIC RING RESONATOR SWITCH FABRICS

I×O	Tested I×O	On-Chip Loss (dB)	Single-Path Crosstalk (dB)	Reference
4×4	2×2	-	−20.8	[24]
4×4	2×4	-	−13.3	[90]
4×4	2×4	17.8	−13.6	[65]
4×4	4×4	-	−10.1	[93]
5×5	1×4	4	−10.3	[92]
5×5	5×5	-	−16	[91]
5×5	5×5	-	−11.3	[94]
1×8	1×8	-	−39	[96]
8×4	1×1	15	−35	[97]
8×7	8×4	10	−19.5	[29]
8×8	2×2	13	-25	[69]

[Lee and Dupuis, *J. Lightw. Technol.* 2019, 37 (1) 6-20]

RR Design Challenges

- Narrowband frequency response
  - ✘ *multiple small rings (large FSR)*
  - ? *one large ring (small FSR)*
  - ? *wavelength routing*
- Tuning ring resonance to grid
  - ✔ *phase tuners for λ alignment*
- Locking ring resonance to wavelength grid
  - ✔ *closed-loop wavelength locking circuits*
- Bandwidth vs. extinction vs. drive tradeoff
  - ✔ *high-order filters using coupled rings*
- Order vs. loss tradeoff
  - ? *balance bandwidth, extinction, loss*
- Electro-optic phase shifter resistance
  - ✘ *Shorter phase shifters have higher series resistance; resulting Joule heating is deleterious to switch performance*

The ONRAMPS Project

For more details, please attend talk M4D.3

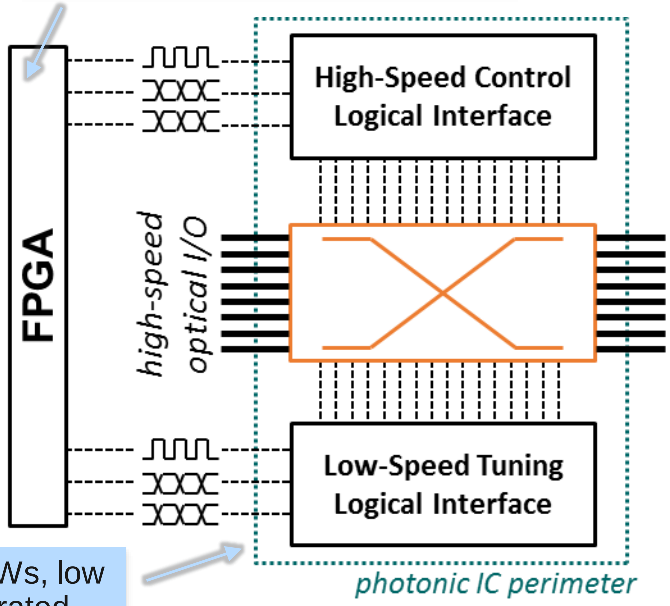
Key Technical Approach

- Dense, energy-efficient, and scalable photonic switch with high per-port bandwidths and nanosecond reconfigurability
- Fabricated and assembled in commercial high-volume manufacturing facilities
- Utilize standard flow for GlobalFoundries 9WG photonic/CMOS process

Key Technical Challenges

- 100s of integrated photonic components → high performance with good uniformity
- 10s of photonic to fiber connections → automated alignment & assembly procedures
- Fast optical switching → a new class of fast control software and hardware

System Integration: Fast scheduling & control hardware enabling packet-scale switching

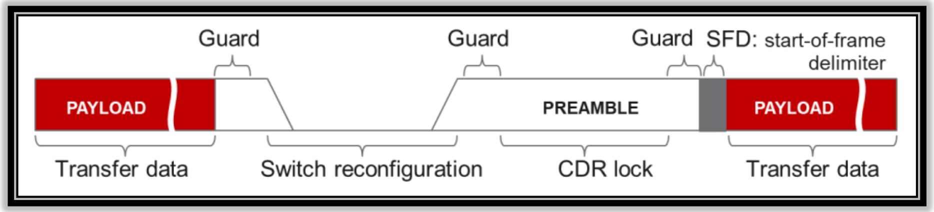


Photonic IC: High port BWs, low power, ns transients, integrated elec's w/ digital interfaces

Packaged Switch Module: Multichannel optical coupling to IC flipped onto laminate using high-volume compatible assembly

Need Fast Control Plane

- Novel control plane required for switch control and link synchronization
- Reconfiguration speeds stress conventional optical circuit switching control methods
- Fast-locking burst-mode data transmission needed in tandem with fast switching
- Initial lab control plane demonstration providing system-level switching time of 60ns achieved [*pending publication*]

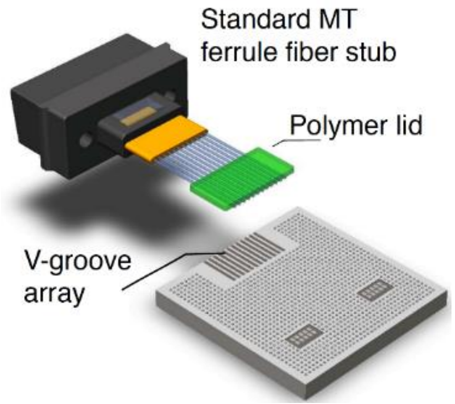


"system-level switching time"

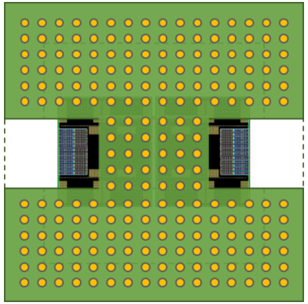
Need High Density Fiber Coupling

Demo'd 12-channel fiber ribbon attached to chip using fiber v-grooves with meta-material spot-size converters

[T. Barwicz, JSTQE 2019, **25** (3), pp. 1-13]



Bottom side of BGA package



Working to extend to packaged chip on high-density laminate with dual-sided multi-fiber couplers

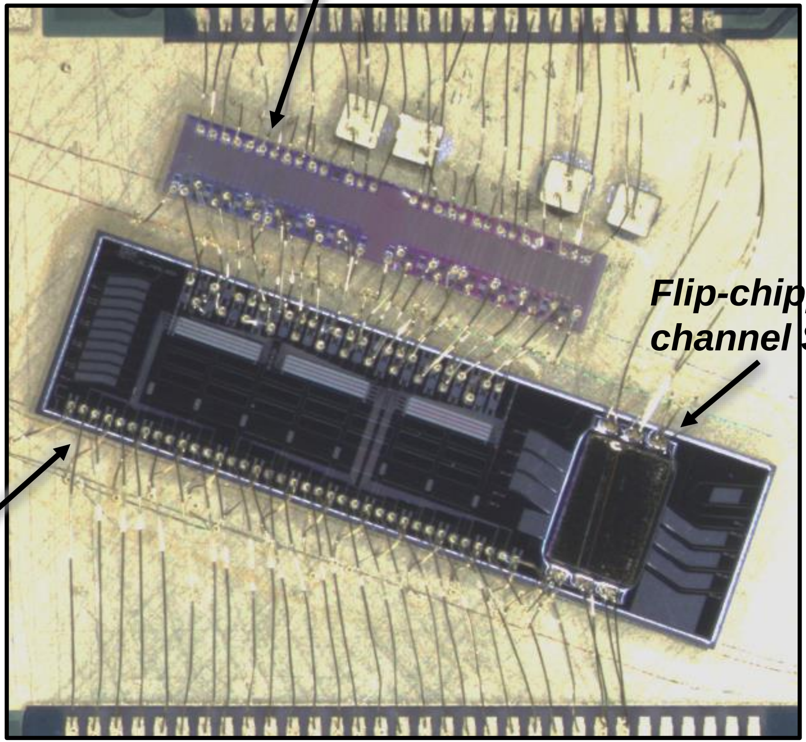
Need for Integrated Optical Amplification

Optical amplification will be needed within the photonic switch platform to compensate loss.

First transparent nanosecond photonic switch to be reported Wednesday

[N. Dupuis *et al.*, W1E.2]

CMOS state controller and digital driver array IC



Flip-chipped InP 4-channel SOA array

Photonics only chip with nanosecond non-blocking 4×4 photonic switch fabric

* Switch and SOA devices funded under DARPA POEM

Summary

- **Electronic switch ASICs will run into thermal limitations**
- **Free-space optical switching faces cost and form factor challenges**
- **Photonic switching solutions offer:**
  - Compared to electronics: Competitive density and cost with improved bandwidth & efficiency
  - Compared to free-space optics: A tradeoff in performance and scalability for lower cost, higher density, and *much* faster reconfigurability
- **Demonstrated integration levels and component performances sufficient for implementing high-performance fabrics**
- **Three approaches: Thermo-optic, Photonic MEMS, Electro-optic**
- **Electro-optic switch fabrics have many hurdles to overcome, but have potential for significant reward**
- **Improvements still needed in polarization-handling, multi-fiber coupling, optical gain integration, and network control**