

**Thin Film
Passive
Components**



TECDIA Co., Ltd.
www.tecdia.com



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General Features

Ceramic Dielectric

Tecdia produces over 95% of the ceramic wafers used to manufacture its capacitors, using fine ceramic powders consisting of unique titanate formulations and proprietary firing processes. A variety of dielectrics are produced from these formulations, covering a range of dielectric constant (K) values, temperature characteristics (TC), and other properties. The products included in this catalog fall within the industry standard dielectric classes I & II. Tecdia also produces EIA class IV single layer ceramic chip capacitors using Grain Boundary Barrier Layer (GBBL) technology.

Electrode Metallization

The sintered wafers are lapped and polished to produce smooth, flat surfaces onto which metal is deposited using dry (sputtering) metallization processes to produce electrodes with ultra-low loss at microwave and millimeter-wave frequencies, and enable reliable thermocompression attachment of gold wires.

Metallization Type	Applicable Metals	Purpose
Diffusion Prevention Layer	TaN	Stop Ti from diffusing Used as resistive material for Integrated Resistor-Capacitor and Thin Film Chip Resistor
Adhesion Layer	TiW or Ti	Create strong bond between metal and ceramic
Barrier Layer	Pt	Protect adhesion layer during solder attach
Conductive Layer	Au	Wire bondable, high conductivity layer

Environmental Commitment

Tecdia's environmental policy is published on our website: www.tecdia.com. Our manufacturing facilities are ISO 14001 certified. All our capacitors are RoHS compliant.

Single Layer Capacitors

Designs

Tecdia Chip Capacitors are normally constructed as square chips for single values and binary capacitor arrays, and in rectangular shapes for capacitor row arrays and custom designs. Tecdia uses variations in chip thickness (by lapping), as well as electrode/ceramic size and dielectric constant to construct capacitors. This permits a broad range of capacitance values to be manufactured with various form factors and designs.

Tecdia has a long history of manufacturing capacitors with bare ceramic margins around the periphery of the electrodes, and has the expertise to produce them in its full range of sizes and values. The borders help prevent short circuits (arcing at the chip edges) after die attachment, especially with conductive epoxy. The design also reduces damage to the electrode when handling with tweezers, and facilitates visual recognition for automated pick and place assembly processes.

Single Layer Capacitors Design Styles

Type A		Type B		Type C	
Top	Border Electrode	Top	Border Electrode	Top	Fully Metallized
Bottom	Fully Metallized	Bottom	Border Electrode	Bottom	Fully Metallized

Single Layer Capacitors Dielectric Specifications

EIA Class ²	Tecdia Dielectric Material Code	Dielectric Constant (Nominal)	Dissipation Factor @ 25 °C	Insulation Resistance @ 25 °C	EIA TC Code ²	Temperature Characteristics	Temperature Range
1	P	40	< 0.15% @ 1 MHz	10 ⁶ MΩ	COG	0 ± 30 ppm / °C	-55 °C to +125 °C
1	4	90	< 0.25% @ 1 MHz	10 ⁶ MΩ	S2H	-330 ± 60 ppm / °C	-55 °C to +125 °C
1	5	140	< 0.25% @ 1 MHz	10 ⁶ MΩ	U2J	-750 ± 120 ppm / °C	-55 °C to +125 °C
1	7	280	< 0.25% @ 1 MHz	10 ⁵ MΩ ¹	M3K	-1000 ± 250 ppm / °C	-55 °C to +125 °C
2	F	1,600	< 2.5% @ 1 kHz	10 ⁵ MΩ	X7R	± 15%	-55 °C to +125 °C
2	C	2,800	< 2.5% @ 1 kHz	10 ⁵ MΩ	X7R	± 15%	-55 °C to +125 °C
4	10	16,000	< 2.5% @ 1 kHz	10 ⁴ MΩ	X7S	± 22%	-55 °C to +125 °C
4	11	30,000	< 2.5% @ 1 kHz	10 ⁴ MΩ	X7S	± 22%	-55 °C to +125 °C
4	12	50,000	< 2.5% @ 1 kHz	10 ⁴ MΩ	X7S	± 22%	-55 °C to +125 °C

Note 1: Minimum 10⁶ MΩ @ 25 °C is available by special order.

Note 2: See EIA-198-1-F.

Screening

Tecdia's capacitors are designed and manufactured for a wide range of applications from high volume commercial communication systems to flight and space programs with stringent quality and performance requirements. The same production processes are used for all our capacitors, whether used for "High Reliability", industrial or commercial applications. However, selection and screening criteria may vary based on procurement requirements. The screening of capacitors falls within three categories: Standard Grade, Commercial Grade, and Custom.

Regular Scheduled Screening For Single Layer Capacitors

Characteristics		Quantity Inspected	Allowable Failures
Visual	Visual Inspection	Inspection Lot AQL II (1.0%)	Inspection Lot AQL II (1.0%)
	Capacitance	Inspection Lot AQL II (1.0%)	Inspection Lot AQL II (1.0%)
Electrical	Dissipation Factor (DF)	Inspection Lot AQL II (1.0%)	Inspection Lot AQL II (1.0%)
	Insulation Resistance (IR)	10 pcs per Wafer Lot* ¹	0* ¹
	Dielectric Withstanding Voltage (DWV)	10 pcs per Wafer Lot	0
Mechanical	Wire Pull	3 pcs per Wafer Lot	0
High Temperature	400 °C For 5 min.	5 pcs per Wafer Lot* ²	0* ²
Dimension Check	Measurement of Capacitor Dimensions	3 pcs per Wafer Lot	0

*¹ Inspection Lot AQL I (0.15%) is applied for Class IV products.

*² Not applicable for class IV products.

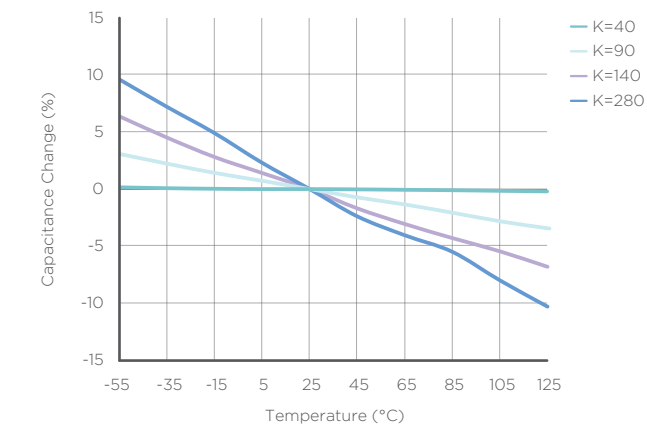
Test Lab Capabilities

Parameter	Test Condition
Temperature Cycling	MIL-STD-883 / Method 1010 Cond. A / B / C
Thermal Shock	MIL-STD-202 / Method 107 Cond. A / B / F
Voltage Conditioning	MIL-STD-883 / Method 1015 Cond. A / B / C / F
Capacitance & DF	MIL-STD-202 / Method 305
IR	MIL-STD-202 / Method 302
DWV	MIL-STD-202 / Method 301
Bond Pull	MIL-STD-883 / Method 2011 Cond. D
Die Shear	MIL-STD-883 / Method 2019 less than 3 kg
Temperature Coefficient Limits	EIA-198 / Method 105
Immersion	MIL-STD-202 / Method 104
Resistance to Solder Heat	MIL-STD-202 / Method 210 Cond. A / B / C / D
Moisture Resistance	MIL-STD-202 / Method 106
Life	MIL-STD-202 / Method 108 less than or equal 150 °C
Humidity (Steady State)	MIL-STD-202 / Method 103
Constant Acceleration	MIL-STD-883 / Method 2001 Cond. A / B / C / D / E / F / G / H / Y1
Vibration	MIL-STD-202 / Method 201
Vibration, High Frequency	MIL-STD-202 / Method 204 Cond. A / B / C / D
Vibration, Variable Frequency	MIL-STD-883 / Method 2007 Cond. A

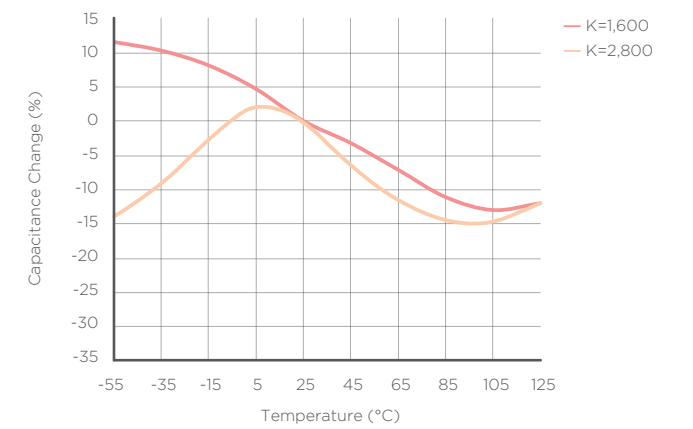
For more information on proper components use, visit our website. Tecdia may, at its discretion, with or without notice and without liability to Tecdia, suspend sales of the products and/or revise product information from that which is published in the Catalog (B-028-2).

Typical Characteristics

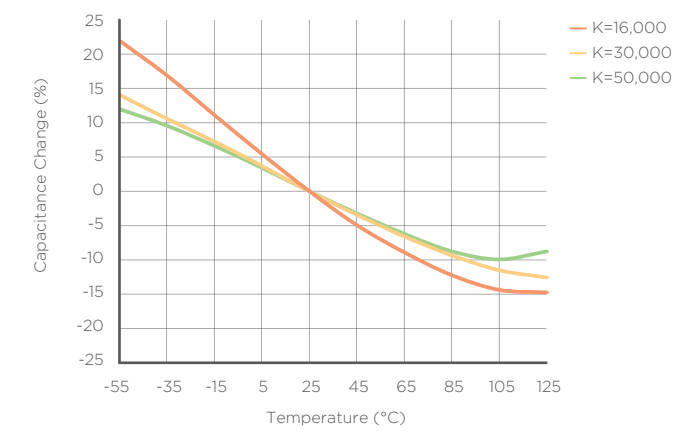
Typical Temperature Characteristics (Class I)



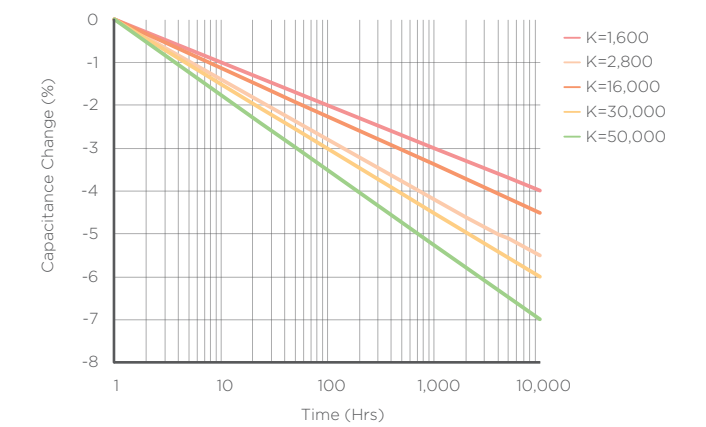
Typical Temperature Characteristics (Class II)



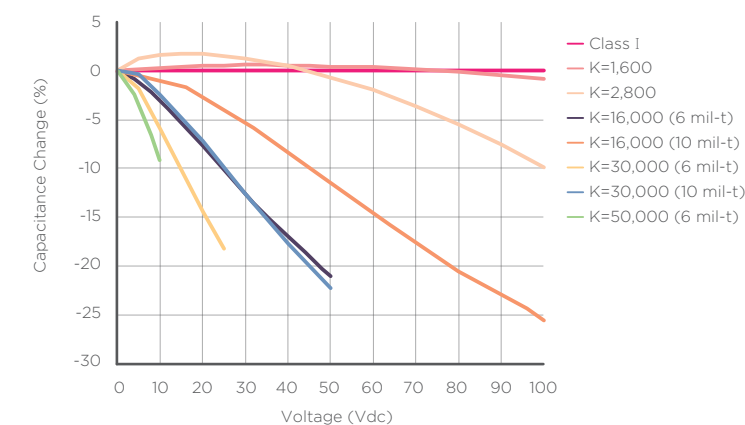
Typical Temperature Characteristics (Class IV)



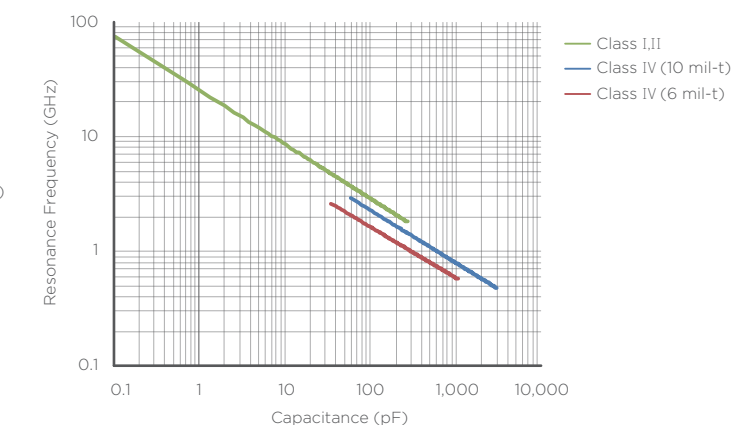
Typical Aging Characteristics



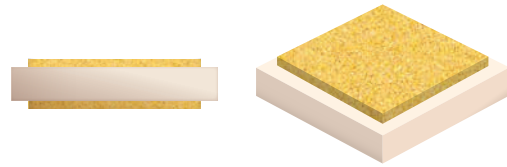
Typical DC Bias Characteristics



Typical Resonance Frequency (GHz)



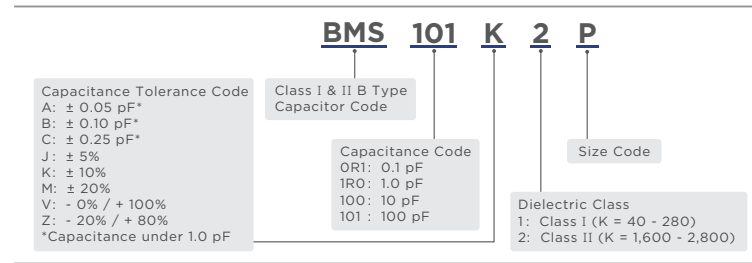
Single Layer Capacitors Type B



Class I & Class II

Class I and II single layer capacitors with borders on top and bottom electrode to aid with visual recognition, preventing shorting due to epoxy creep up, and possessing top-bottom symmetry.

Electrode Metallization Scheme	
Top	TiW - Au, TaN - TiW - Au
Bottom	TiW - Au, TaN - TiW - Au



Selection Guide

Size Code		B	C	F	H	K	P	R	S	T
Size L x W	mils	10 x 10	12 x 12	16 x 16	20 x 20	24 x 24	31 x 31	40 x 40	50 x 50	60 x 60
Cap (pF)	Cap Code	0.25 x 0.25	0.30 x 0.30	0.40 x 0.40	0.50 x 0.50	0.60 x 0.60	0.8 x 0.8	1.00 x 1.00	1.25 x 1.25	1.50 x 1.50
0.1	OR1									
0.2	OR2									
0.3	OR3									
0.4	OR4									
0.5	OR5									
0.6	OR6									
0.8	OR8									
1	1R0									
1.2	1R2									
1.5	1R5									
1.8	1R8									
2.2	2R2									
2.7	2R7									
3.3	3R3									
3.9	3R9									
4.7	4R7									
5.6	5R6									
6.8	6R8									
8.2	8R2									
10	100									
12	120									
15	150									
18	180									
22	220									
27	270									
33	330									
39	390									
47	470									
50	500									
56	560									
68	680									
82	820									
100	101									
120	121									
150	151									
180	181									
220	221									
270	271									
330	331									
390	391									
470	471									
510	511									

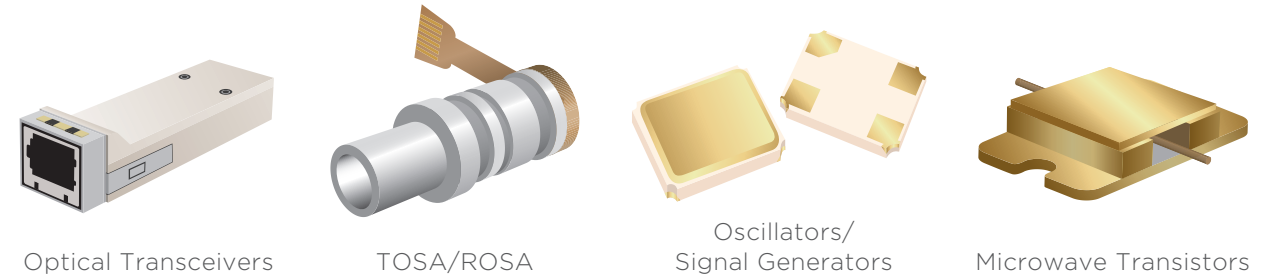
Note: Manufactured to metric dimensions. Imperial units are for reference only.



Application Notes

Tecdia's SLCs are used in a variety of devices in the optical and RF market including, but not limited to,

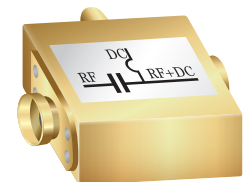
- Microwave/Optical Transceivers
- Synthesizers, Oscillators and other signal generators
- TOSA/ROSA/BOSA (Transmit/Receive/Bidirectional Optical Sub-Assemblies)
- Microwave/Optical Amplifiers and Modulators
- High Frequency Signal and RF Measurement Equipment



In these devices SLC function can be summarized into the 3 categories; DC Block, High Frequency Bypass and Impedance Matching.

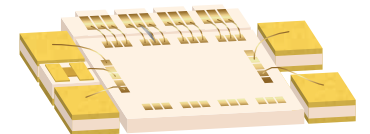
DC Block

In the DC Block application, the chip capacitor is placed in series in a circuit to prevent the DC bias voltage from one circuit from affecting another. The capacitance is chosen so that the capacitor approximates a short at the frequency of interest.



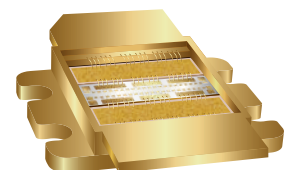
High Frequency Bypass

In the High Frequency Bypass application, the chip capacitor is placed in shunt (ground) within a circuit to remove high frequency noise or signals by shorting them to ground. The capacitance is chosen such that high frequencies see a low impedance path to ground, while the DC bias voltage or lower frequency signals see a high impedance path to ground and can hence continue along the circuit with minimal attenuation.

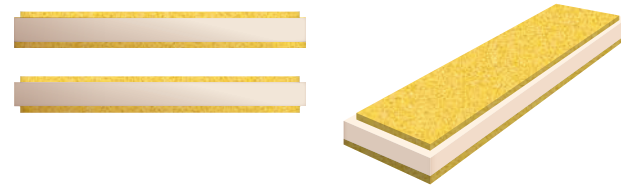


Impedance Matching

The Impedance Matching application uses a chip capacitor to provide a specific reactance in a circuit to achieve the desired impedance. These capacitors can be used in numerous lumped circuits to minimize reflections and maintain the signal when passing through elements/circuits of different impedances.

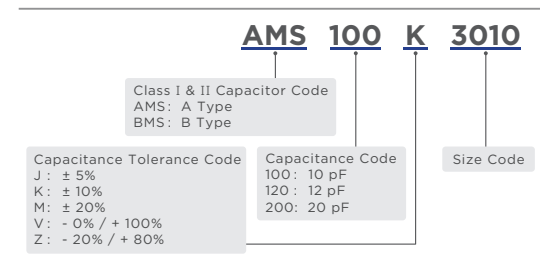


Rectangular Capacitors



Tecdia has a range of high-aspect ratio rectangular capacitors available, popular for use in GaN matched transistor packages.

Electrode Metallization Scheme	
Top	TiW - Au, TaN - TiW - Au
Bottom	TiW - Pt - Au, TaN - TiW - Pt - Au, TiW - Au, TaN - TiW - Au



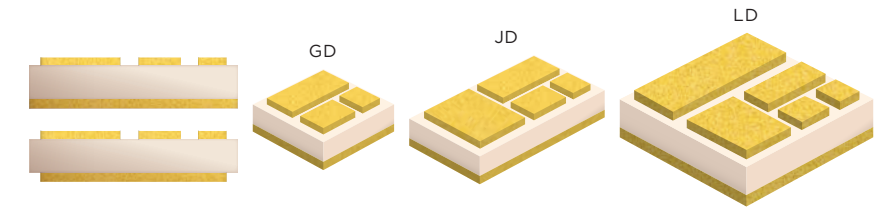
Standard Parts

Part Number	Capacitance (pF)	Size (mils) L x W x t	Size (mm) L x W x t	Dielectric	RWV
AMS100K3010	10	118 x 39 x 8	3.0 x 1.0 x 0.20	K = 90	80 V
AMS120K3010	12	118 x 39 x 7	3.0 x 1.0 x 0.17	K = 90	80 V
AMS140K3010	14	118 x 39 x 7	3.0 x 1.0 x 0.18	K = 130	80 V
AMS160K3010	16	118 x 39 x 7	3.0 x 1.0 x 0.17	K = 130	80 V
AMS180K3010	18	118 x 39 x 6	3.0 x 1.0 x 0.15	K = 130	80 V
AMS200K3010	20	118 x 39 x 5	3.0 x 1.0 x 0.13	K = 130	80 V
AMS100K6010	10	236 x 39 x 7	6.0 x 1.0 x 0.19	K = 40	80 V
AMS120K6010	12	236 x 39 x 7	6.0 x 1.0 x 0.18	K = 40	80 V
AMS210K6010	21	236 x 39 x 8	6.0 x 1.0 x 0.20	K = 90	80 V
AMS240K6010	24	236 x 39 x 7	6.0 x 1.0 x 0.17	K = 90	80 V
AMS260K6010	26	236 x 39 x 6	6.0 x 1.0 x 0.16	K = 90	80 V
AMS300K6010	30	236 x 39 x 7	6.0 x 1.0 x 0.19	K = 130	80 V
AMS350K6010	35	236 x 39 x 7	6.0 x 1.0 x 0.17	K = 130	80 V
AMS400K6010	40	236 x 39 x 7	6.0 x 1.0 x 0.17	K = 130	80 V
AMS450K6010	45	236 x 39 x 5	6.0 x 1.0 x 0.13	K = 130	80 V
AMS500K6010	50	236 x 39 x 4	6.0 x 1.0 x 0.11	K = 130	80 V

If you have custom specifications you wish to satisfy then Tecdia can tailor the dimensions, dielectric constant, capacitance, TC and other options to match any particular die form factor you are using.

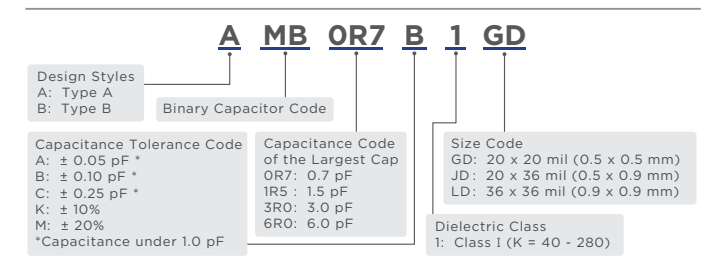
Note 1: Manufactured to metric dimensions. Imperial units are for reference only.
 Note 2: Typical resonance frequency on page 4 does not apply to this product line.

Binary Capacitors



Binary Capacitors are available in arrays with 3, 4 or 5 electrodes that share a common rear electrode, convenient for tuning the capacitance to be used in circuits.

Electrode Metallization Scheme	
Top	TiW - Au, TaN - TiW - Au
Bottom	TiW - Pt - Au, TaN - TiW - Pt - Au, TiW - Au, TaN - TiW - Au



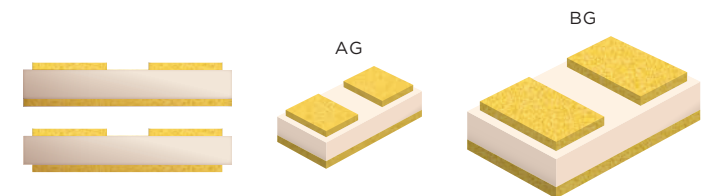
Standard Parts

Part Number	Capacitance Code of the Largest Cap	Array Pad Capacitance (pF)	Size (mils) L x W	Size (mm) L x W	Dielectric
AMB0R7B1GD	OR7	0.7 / 0.35 / 0.18	20 x 20	0.5 x 0.5	K = 140
BMB0R7B1GD	OR7	0.7 / 0.35 / 0.18	20 x 20	0.5 x 0.5	K = 140
AMB1R5K1GD	1R5	1.5 / 0.75 / 0.38	20 x 20	0.5 x 0.5	K = 280
BMB1R5K1GD	1R5	1.5 / 0.75 / 0.38	20 x 20	0.5 x 0.5	K = 280
AMB1R5K1JD	1R5	1.5 / 0.75 / 0.38 / 0.19	20 x 36	0.5 x 0.9	K = 140
BMB1R5K1JD	1R5	1.5 / 0.75 / 0.38 / 0.19	20 x 36	0.5 x 0.9	K = 140
AMB3R0K1JD	3R0	3.0 / 1.5 / 0.75 / 0.38	20 x 36	0.5 x 0.9	K = 280
BMB3R0K1JD	3R0	3.0 / 1.5 / 0.75 / 0.38	20 x 36	0.5 x 0.9	K = 280
AMB3R0K1LD	3R0	3.0 / 1.5 / 0.75 / 0.38 / 0.19	36 x 36	0.9 x 0.9	K = 140
BMB3R0K1LD	3R0	3.0 / 1.5 / 0.75 / 0.38 / 0.19	36 x 36	0.9 x 0.9	K = 140
AMB6R0K1LD	6R0	6.0 / 3.0 / 1.5 / 0.75 / 0.38	36 x 36	0.9 x 0.9	K = 280
BMB6R0K1LD	6R0	6.0 / 3.0 / 1.5 / 0.75 / 0.38	36 x 36	0.9 x 0.9	K = 280

Binary relationship is based on the relative sizes (surface area) of the electrodes within the array instead of the actual electrical values for the individual capacitors. Screening Acceptance Procedures are based on measurements of the largest electrode pad only.

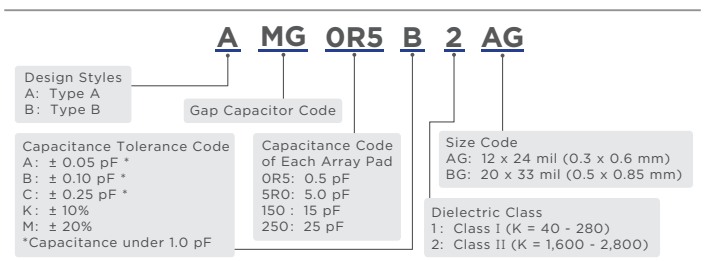
Note 1: Manufactured to metric dimensions. Imperial units are for reference only.
 Note 2: Typical resonance frequency on page 4 does not apply to this product line.

Gap Capacitors



Gap Capacitors are constructed on a single rectangular chip, with two electrodes on the same surface providing a series connection when mounted array side down, eliminating bonding wire inductance.

Electrode Metallization Scheme	
Top	TiW - Au, TaN - TiW - Au
Bottom	TiW - Pt - Au, TaN - TiW - Pt - Au, TiW - Au, TaN - TiW - Au

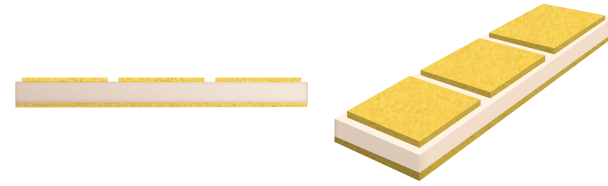


Standard Parts

Part Number	Capacitance Code of Each Array Pad	Capacitance Mounted (pF)	Size (mils) L x W	Size (mm) L x W	Dielectric
AMG0R5B1AG	OR5	0.25	12 x 24	0.3 x 0.6	K = 140
BMG0R5B1AG	OR5	0.25	12 x 24	0.3 x 0.6	K = 140
AMG5R0K2AG	5R0	2.5	12 x 24	0.3 x 0.6	K = 1,600
BMG5R0K2AG	5R0	2.5	12 x 24	0.3 x 0.6	K = 1,600
AMG150K2BG	150	7.5	20 x 33	0.5 x 0.85	K = 1,600
BMG150K2BG	150	7.5	20 x 33	0.5 x 0.85	K = 1,600
AMG250K2BG	250	12.5	20 x 33	0.5 x 0.85	K = 2,800
BMG250K2BG	250	12.5	20 x 33	0.5 x 0.85	K = 2,800

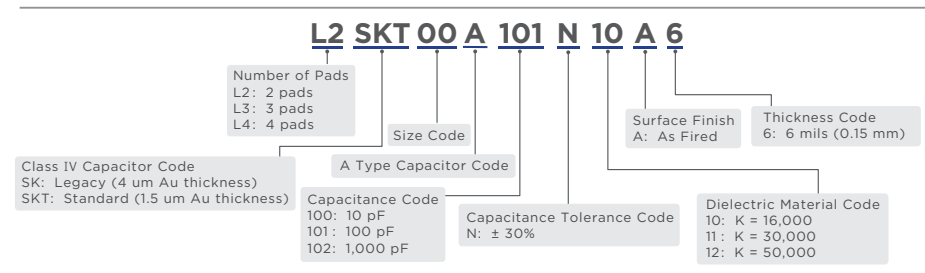
Note 1: Manufactured to metric dimensions. Imperial units are for reference only.
 Note 2: Typical resonance frequency on page 4 does not apply to this product line.

Row Capacitors



An array of 2 or more Type A capacitors onto a single chip for increased capacitance density, fewer components to place and optimal packing efficiency.

Electrode Metallization Scheme	
Top	TiW - Au, Ti - TiW - Au
Bottom	Ti - Pt - Au



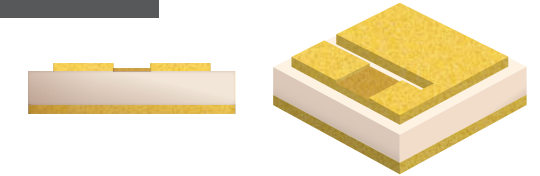
Selection Guide
Thickness: 6 mils ± 1 mil (0.15 mm ± 0.025 mm)

Size Code		00	01	02	03	04	
2 Pads	Size L x W	mils	20 x 10	30 x 15	40 x 20	50 x 25	60 x 30
		Tolerance	± 4 x ± 2	± 4 x ± 2	± 4 x ± 4	± 6 x ± 4	± 8 x ± 4
mm		0.50 x 0.25	0.76 x 0.38	1.00 x 0.50	1.27 x 0.63	1.52 x 0.76	
Tolerance		± 0.10 x ± 0.05	± 0.10 x ± 0.05	± 0.10 x ± 0.10	± 0.15 x ± 0.10	± 0.20 x ± 0.10	
3 Pads	Size L x W	mils	30 x 10	45 x 15	60 x 20	75 x 25	90 x 30
		Tolerance	± 4 x ± 2	± 5 x ± 2	± 8 x ± 4	± 8 x ± 4	± 10 x ± 4
mm		0.76 x 0.25	1.14 x 0.38	1.52 x 0.50	1.90 x 0.63	2.28 x 0.76	
Tolerance		± 0.10 x ± 0.05	± 0.12 x ± 0.05	± 0.20 x ± 0.10	± 0.20 x ± 0.10	± 0.25 x ± 0.10	
4 Pads	Size L x W	mils	40 x 10	60 x 15	80 x 20	100 x 25	120 x 30
		Tolerance	± 6 x ± 2	± 6 x ± 2	± 8 x ± 4	± 10 x ± 4	± 12 x ± 4
mm		1.00 x 0.25	1.52 x 0.38	2.00 x 0.50	2.54 x 0.63	3.04 x 0.76	
Tolerance		± 0.15 x ± 0.05	± 0.15 x ± 0.05	± 0.20 x ± 0.10	± 0.25 x ± 0.10	± 0.30 x ± 0.10	
Cap (pF)	Cap Code						
82	820						
100	101						
120	121						
150	151						
180	181						
220	221						
270	271						
330	331						
390	391						
470	471						
560	561						
680	681						
820	821						
1000	102						
1200	122						
1500	152						
1800	182						

Note 1: Manufactured to metric dimensions. Imperial units are for reference only.
 Note 2: Typical resonance frequency on page 4 does not apply to this product line.
 Note 3: Electrical characteristics are measured between top and bottom electrodes only.
 No bias voltage should be applied between electrodes on top surface.

Dielectric Material	K = 16,000	K = 30,000	K = 50,000
Rated Working Voltage	50 V	16 V	10 V

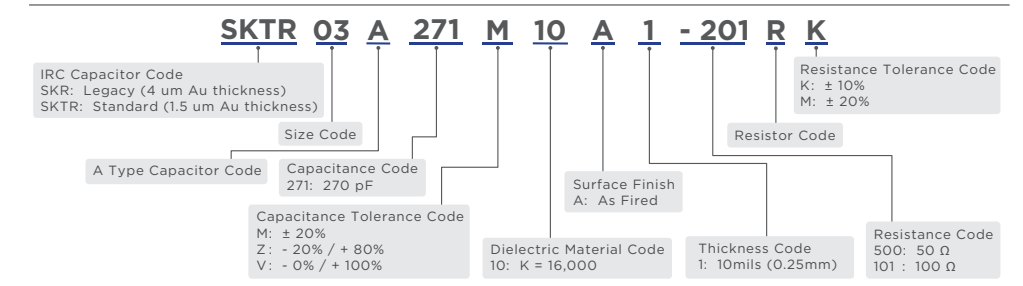
Integrated Resistor-Capacitors (IRC™)



Integration of a resistor onto a capacitor to form a single ceramic chip made with Tecdia's Class IV (K=16,000) dielectric, decreasing BOM count and requiring one less wire bond.

Electrode Metallization Scheme

Top	TaN - TiW - Au
Bottom	Ti - Pt - Au



Selection Guide
Thickness: 10 mils ± 1 mil (0.250 mm ± 0.025 mm)

Size Code		03	04	05	06	64	65
Size L x W	mils	25 x 25	30 x 30	35 x 35	40 x 40	40 x 30	40 x 35
	Tolerance	± 5 x ± 5	± 5 x ± 5	± 5 x ± 5	± 5 x ± 5	± 5 x ± 5	± 5 x ± 5
	mm	0.63 x 0.63	0.76 x 0.76	0.88 x 0.88	1.00 x 1.00	1.00 x 0.76	1.00 x 0.88
	Tolerance	± 0.13 x ± 0.13	± 0.13 x ± 0.13	± 0.13 x ± 0.13	± 0.13 x ± 0.13	± 0.13 x ± 0.13	± 0.13 x ± 0.13
Cap (pF)	Cap Code						
220	221						
270	271	*					
330	331						
390	391						
470	471						
560	561						
680	681				*		+
Resistance (Ω)	Resistance Code						
50	500						
100	101	**	**	**	**	**	**
200	201	**	**	**	**	**	**

* Capacitance tolerance V is not applicable.

Dielectric Material	K = 16,000
Rated Working Voltage	100 V

Temperature Characteristic of Resistance (TCR)
- 100 ± 50 ppm / °C (@ - 55 °C to + 85 °C)

Resistor Rated Power
100 mW @ < 70 °C
70 mW @ < 85 °C
**50 mW @ < 70 °C
**35 mW @ < 85 °C

Heat Resistance
320 °C x 5 minutes N₂ atmosphere

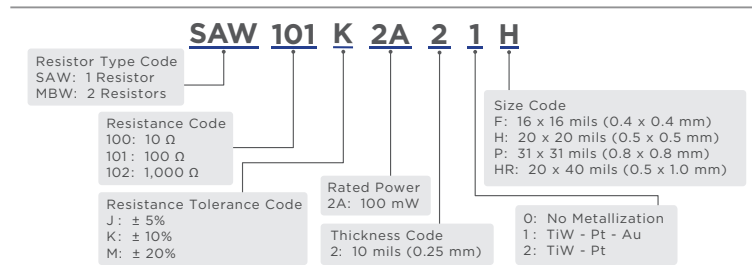
Note 1: Manufactured to metric dimensions. Imperial units are for reference only.
 Note 2: Typical resonance frequency on page 4 does not apply to this product line.

Thin Film Chip Resistors



Wire-bondable chip resistors for biasing, RF line termination, and various other applications.

Electrode Metallization Scheme	
Top	TaN - TiW - Au
Bottom	TiW - Pt - Au



Standard Parts

Part Number	Resistance (Ω)	Resistance Code	Size (mils) L x W	Size (mm) L x W	Configuration
SAW100K2A21H	10	100	20 x 20	0.50 x 0.50	SA Series - 1
SAW250K2A21F	25	250	16 x 16	0.40 x 0.40	SA Series - 1
SAW250K2A21H	25	250	20 x 20	0.50 x 0.50	SA Series - 1
SAW500K2A21F	50	500	16 x 16	0.40 x 0.40	SA Series - 1
SAW500K2A21H	50	500	20 x 20	0.50 x 0.50	SA Series - 1
SAW500K2A21HR	50	500	20 x 40	0.50 x 1.00	SA Series - 1
SAW500K2A21P	50	500	31 x 31	0.80 x 0.80	SA Series - 1
SAW750K2A21HR	75	750	20 x 40	0.50 x 1.00	SA Series - 1
SAW101K2A21H	100	101	20 x 20	0.50 x 0.50	SA Series - 1
SAW101K2A21HR	100	101	20 x 40	0.50 x 1.00	SA Series - 1
SAW201K2A21H	200	201	20 x 20	0.50 x 0.50	SA Series - 2
SAW102M2A21H	1000	102	20 x 20	0.50 x 0.50	SA Series - 3
MBW200K2A21P	10 x 2	200	31 x 31	0.80 x 0.80	MB Series
MBW250K2A21P	12.5 x 2	250	31 x 31	0.80 x 0.80	MB Series
MBW500K2A21P	25 x 2	500	31 x 31	0.80 x 0.80	MB Series
MBW750K2A21P	37.5 x 2	750	31 x 31	0.80 x 0.80	MB Series
MBW101K2A21P	50 x 2	101	31 x 31	0.80 x 0.80	MB Series

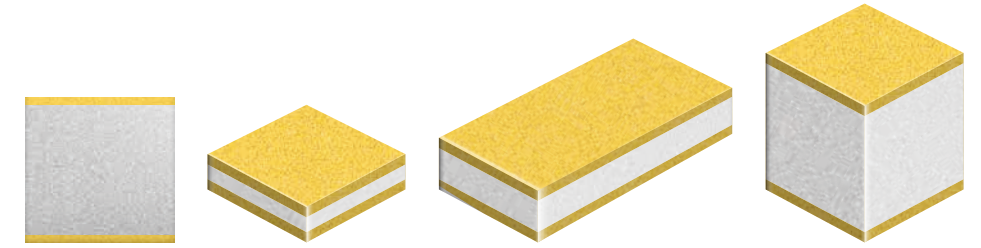
Note: Manufactured to metric dimensions. Imperial units are for reference only.

Temperature Characteristic of Resistance (TCR)
- 100 + / - 50 ppm / °C (@ - 55 °C to + 85 °C)

Resistor Rated Power
100 mW @ < 70 °C

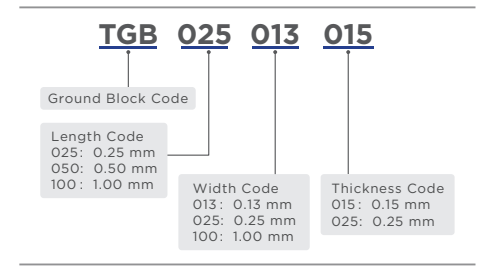
Heat Resistance
320 °C x 5 minutes N2 atmosphere

Ground Blocks



Tecdia Ground Blocks are customizable conductive ceramic shims ideal for application within micro-assemblies in both optical and microwave industries.

Electrode Metallization Scheme	
Top	Ti - Pt - Au
Bottom	Ti - Pt - Au



Standard Parts

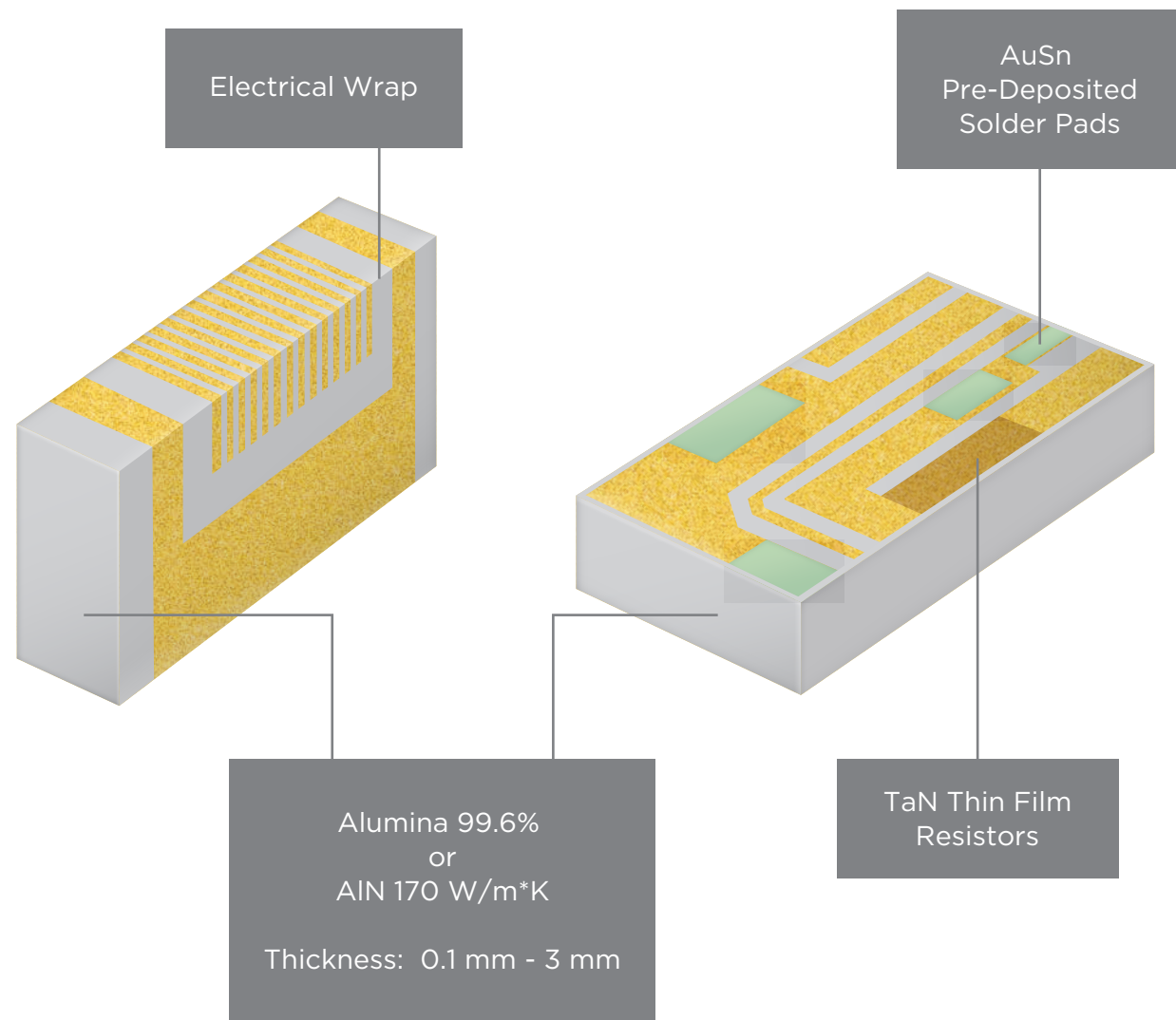
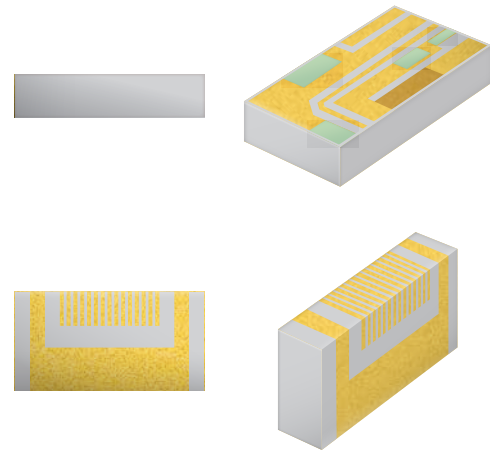
Part Number	Size (mils) L x W x t	Size (mm) L x W x t
TGB025013015	10 x 5 x 6	0.25 x 0.13 x 0.15
TGB025025015	10 x 10 x 6	0.25 x 0.25 x 0.15
TGB025013025	10 x 5 x 10	0.25 x 0.13 x 0.25
TGB025025025	10 x 10 x 10	0.25 x 0.25 x 0.25
TGB050013015	20 x 5 x 6	0.50 x 0.13 x 0.15
TGB050025015	20 x 10 x 6	0.50 x 0.25 x 0.15
TGB050050015	20 x 20 x 6	0.50 x 0.50 x 0.15
TGB050013025	20 x 5 x 10	0.50 x 0.13 x 0.25
TGB050025025	20 x 10 x 10	0.50 x 0.25 x 0.25
TGB050050025	20 x 20 x 10	0.50 x 0.50 x 0.25

Custom Part Design Guide

Parameter	Specification
Length: L	0.25 mm - 2.00 mm
Width: W	0.13 mm - 2.00 mm
Thickness: t	0.08 mm - 0.63 mm
Resistivity	3 x 10 ⁻⁵ Ωm nominal

Thin Film Ceramic Substrates

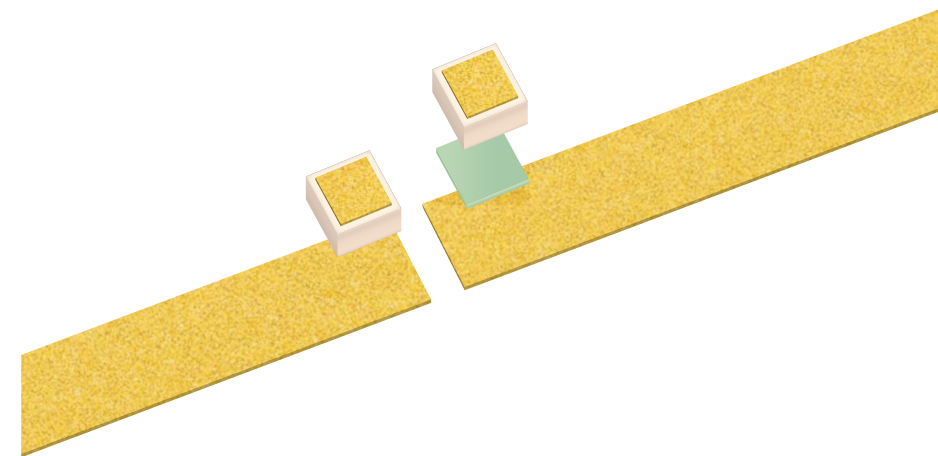
Tecdia's Thin Film Substrates technologies combine over 40 years of experience in ceramics, machining, wafer processing, and thin film metallization techniques into one group that specializes in build-to-print thin film metallized ceramic substrates. Features such as fine patterns, electrical wraps, thin film resistors and pre-deposited AuSn are all specialized for miniaturized high-speed communication devices.



Single Layer Capacitors Options

Predeposited AuSn

AuSn (gold-tin solder) can be added to the metallization stack of any type A (top border only) or type C (no borders) Tecdia capacitors for easier and faster eutectic die attach process.



No Backside Gold

No back side gold capacitors have no Au in the backside metallization stack. The absence of gold helps decrease overall costs, but makes the capacitor only compatible with epoxy attachment.

Packaging

Packaging

Standard Packaging

	Material	Color	Size
Waffle Pack	ABS	White / Natural	2 inch

Customized Packaging

	Material	Color	Size
Waffle Pack*	Conductive PC	Black	2 inch
Blue tape (w/Ring)	PVC	Blue	Ø 6 inch
Blue tape (w/o Ring)	PVC	Blue	7.87 inch

*Please contact us if you have special requests for the tray pocket sizes.