ethernet alliance

Higher Speed Ethernet Interoperability – A New Plugfest
By Kent Lusted, Ethernet Alliance Board of Directors; Intel

Ethernet Specifications and Standards Making Progress
Here we are, four months into a new year, and there has already been much activity in the higher speed networking Ethernet ecosystem. The list of the accomplishments in this space includes, but is not limited to the following:

- The IEE 802.3cu-2021™ for 100 Gb/s and 400 Gb/s operation over Single-Mode Fiber specification was published
- The IEEE 802.3ct™ 100 Gb/s over DWDM systems Task Force entered IEEE-SA ballot
- The IEEE P802.3db™ 100 Gb/s, 200 Gb/s, and 400 Gb/s Short Reach Fiber Task Force adopted baselines
- The IEEE P802.3ck™ 100 Gb/s, 200 Gb/s, and 400 Gb/s Electrical Interfaces Task Force entered Working Group ballot
- The IEEE 802.3™ Beyond 400 Gb/s Ethernet Study Group was formed
- The QSFP-DD800 MSA announces an initial hardware specification
- Several SNIA Transceiver subgroup specifications were updated

As I wrote in my last post, I firmly believe that "interoperability is the foundation of Ethernet and makes Ethernet the ubiquitous fabric of choice." Now is the time to reassess compatibility among the various vendors, sub-components and implementations through compliance and interoperability test suites.

Higher Speed Ethernet Plugfest
The Ethernet Alliance Higher Speed Networking (HSN) Subcommittee is pleased to announce our next plugfest scheduled for October 2021 at the UNH InterOperability Laboratory. This interoperability event will be the first to look at 100 Gbps/lane Ethernet electrical PHYs and electrical interfaces and will also revisit 50 Gbps/lane technology. These two lane rates will not only spur the increased use of 100/200/400GbE, but are also key catalysts for moving to the next higher Ethernet rates.

The October 2021 Ethernet Alliance HSN Plugfest is expected to address many different elements of the Ethernet industry, including OSFP, QSFP, QSFP-DD, and SFP connector form factors, in addition to Ethernet switches, FPGAs and NICs, electrical and optical interconnect products, test and measurement equipment, and electrical and optical testing methodologies. An outcome of this HSN Plugfest will be to provide Ethernet developers, operators, and users with the current status on new implementations of the individual building blocks as well as the complete end-to-end solution. Feedback from the event's successes, challenges, and opportunities will be fed back into products as well as the standards development process.

Joining Forces for Interoperability
The Ethernet Alliance HSN subcommittee will be developing the test suites and test criteria for the October 2021 HSN Plugfest in the coming months and actively seeks input and feedback from the industry. Offering a competitive advantage exclusively for members, Ethernet Alliance plugfests provide a neutral, secure testing environment.

If your organization is interested in participating in the plugfest and is not yet a member of the Ethernet Alliance, please reach out to the Ethernet Alliance administration, myself or Pavel Zivny. Don't delay, it will be an exciting and informative event!

Bio:

Kent Lusted co-chairs the Ethernet Alliance High Speed Networking subcommittee. He joined Intel in 1999, focused on designing Ethernet board products and teaching IEEE 802.3 BASE-T compliance testing to customers all over the world. Kent won an Intel Achievement Award in 2002 for his contributions towards delivering the world's first client and dual-port server Gigabit Ethernet controllers. He continues to be an integral part of the Ethernet PHY interoperability debug team over many generations of SERDES products (10 Gbps, 25 Gbps, 50 Gbps and beyond). Since 2012, Kent has been an active contributor and member of the IEEE 802.3 Ethernet PHY standards development leadership team and is currently the Vice-Chair of the IEEE 802.3ck 100G SERDES electrical interfaces Task Force.