

Analog Design Engineer

(junior or senior)

Location: Shanghai, Shenzhen China

Job Responsibilities:

1. Design, analyze and implement high-performance (>10GHz) PLL, wireline amplifiers, CDR, SERDES, PLL, PAM4, TDCs, TOF, low-noise amplifiers, transmitters, power-amplifiers and power-drivers, or other baseband circuits like LDO, temp sensor, ADC, Filters, etc.
2. The design of high-frequency (multi-gigahertz) and high-precision clocking and analog circuits.
3. Use EDA tools (Cadence, Mentor) to run simulation and function verification.
4. Guide layout engineer to optimize layout.
5. Chip debug and testing individually and with the team.
6. Other tasks assigned by line manager.

Qualifications:

1. MSEE or PhD with at least 1 year experience. Excellent fresh graduates are considered.
2. Hands-on design experience
3. Experience in Cadence EDA tools.
4. Team player with good communication skills.
5. Experience with multi-gigahertz high-speed interface like SERDES transmitter/receiver, or TIA/PLL/CDR/LNA, ToF, Temperature Sensor, high-precision/high-speed ADC or power management IC is highly preferred.
6. Experience in Cadence EDA tools.
7. Team player with good communication skills.

Contact: Isabel, Wechat:496912537

Analog Design Manager

Location: Shanghai, Shenzhen China

Job Responsibilities:

1. Lead RD team to design, analyze and implement high-performance (>10GHz) PLL, wireline amplifiers, CDR, SERDES, PLL, PAM4, TDCs, TOF, low-noise amplifiers, transmitters, power-amplifiers and power-drivers, or other baseband circuits like LDO, temp sensor, ADC, Filters, etc.
2. The design of high-frequency (multi-gigahertz) and high-precision clocking and analog circuits.
3. Use EDA tools (Cadence, Mentor) to run simulation and function verification.
4. Guide layout engineer to optimize layout.
5. Chip debug and testing individually and with the team.
6. Other tasks assigned by line manager.

Qualifications:

1. MSEE or PhD with at least 5-year experience.
2. Hands-on design experience.
3. Great team management skills.
4. Experience in Cadence EDA tools.
4. Team player with good communication skills.
5. Experience with multi-gigahertz high-speed interface like SERDES transmitter/receiver, or TIA/PLL/CDR/LNA, ToF, Temperature Sensor, high-precision/high-speed ADC or power management IC is highly preferred.
6. Experience in Cadence EDA tools.
7. Team player with good communication skills.

Senior Analog Layout Engineer

Location: Shanghai China

Job Responsibilities:

1. You will optimize the layout and high-frequency (multi-gigahertz) routing of high-precision analog circuits, such as: high-speed amplifiers, wireline SERDES, PLL, or other baseband circuits like LDO, temp sensor, ADC, Filters, etc.
2. Use EDA tools (Cadence, Mentor, Allegro) to layout, extract, and verify the high-performance layout.
3. Work and iterate with analog/RF engineers to optimize the layout performance.
4. Other tasks assigned by line manager.

Qualifications:

1. BSEE in analog IC design with at least 5-year experience.
2. Experience in Cadence EDA tools.
3. Desired: Experience with the layout of SERDES transmitter/receiver, PLL, TIA, CDR, LNA etc.
4. Desired: Experience in RF circuit layout, including high-frequency effects, crosstalk, and bandwidth optimization.
5. High-voltage BCD is a plus
6. Team player with good communication skills.

Digital Verification Engineer

(junior or senior)

Location: Shanghai, Shenzhen China

Job Responsibilities:

1. This position is for a digital-ASIC verification engineer to build next-generation analog/mixed-signal SoC chipsets.
2. Responsible for all aspects of UVM (Universal Verification Methodology), from start to finish. Good knowledge of communication protocols and associated verification IPs (VIPs). Extensive experience with assertions, cover properties, constrained random testing.
3. Work with other digital designers to verify many aspects of ASIC design flow including: architecture, RTL coding/Verification, Synthesis, DFT, STA and P&R (for backend designer).
4. Participate in chip debug, validation, and marketing specifications.

Qualifications:

1. BSEE and above with at least 3-year verification experience.
2. REQUIRED: Experience in metrics-driven verification methodology (System-Verilog/UVM based).
3. Excellent knowledge of ASIC design, such as arithmetic structure (addition, multiplication, interaction), timing analysis, DFT, meta-stability, etc.
4. Fundamental understanding of digital signal processing, such as FIR/IIR filter structure, error correction, and decimation.
5. Desired usage experience of mainstream industry-standard EDA tools, such as VCS/NC, Design Compiler, PrimeTime, Formality/ Conformal and Tetramax/DFT compiler.
6. Experience in other vertical aspects of ASIC design (front-end and back-end) will be a great plus.
7. Experience in Perl/Python/tcl scripts is a plus.

Contact: Isabel, Wechat:496912537

Digital SOC Design Engineer

(junior or senior)

Location: Shanghai, Shenzhen China

Job Responsibilities:

1. This position is for a digital-SoC/ASIC design engineer to build next-gen analog/mixed-signal SoC chipsets.
2. Handle several aspects of ASIC SoC design flow, which may include: MCU optimization, RTL coding, Verification, Synthesis, DFT, STA and P&R (for back-end design).
3. Participate in chip debug, validation, and marketing specifications.

Qualifications:

1. MSEE with 3-year experience of digital SOC experience.
2. Highly desired is previous experience with MCU instantiation, on-chip memory optimization, P&R, and programming (i.e. ARM Cortex-M0, RISC-V, MIPS).
3. Excellent knowledge of ASIC design, such as arithmetic structure (addition, multiplication), timing analysis, DFT, meta-stability, finite state machines.
4. Fundamental understanding of digital signal processing, such as FIR/IIR filter structure, error correction, integration/averaging, and decimation.
5. Desired usage experience of mainstream industry-standard EDA tools, such as VCS/NC, Design Compiler, PrimeTime, Formality/ Conformal and Tetramax/DFT compiler.
6. Experience in several vertical aspects of ASIC design (front-end and back-end P&R) will be a great plus.
7. Experience in bus design (I2C, AHB/APB/AXI), datapath design (Filter, correlation or Cordic) and logic control (PCS or MAS) is a plus.
8. Experience with CMOS image sensors (digital-design) such as MIPI, readout, and timing control, is a plus.
9. Experience in metrics-driven verification methodology (System-Verilog/UVM based) is a plus.
10. Experience in mixed-signal SOC design is a plus.
11. Experience in perl/python/tcl scripts is a plus.

Contact: Isabel, Wechat:496912537

Physical Design Engineer

(junior or senior)

Location: Shanghai, Shenzhen China

Job Responsibilities:

1. Perform backend design including floor planning, place and routing, timing optimization, and final DRC/LVS.
2. Perform Low Power design/power analysis/formal verification/STA-ECO flow.
3. Solve deep sub-micron design problems such as leakage, power, signal integrity, timing closure, DRC/DFM etc.
4. Develop Perl/TCL/Shell scripts to enhance IC physical design flow and methodology.
5. Other tasks assigned by line manager.

Qualifications:

1. BSEE, MSEE or higher.
2. 3-year experience of large ASIC backend designs.
3. Experience with Synopsys and/or Cadence design tools.
4. Familiar with 45/40nm or lower CMOS process designs.
5. Having successful tape out experience will be a great plus.
6. Good communication skills, team spirit and be anxious to learn during daily work.

For Sales, FAE, DVT, Marketing and other positions, please contact HR-Isabel (wechat: 496912537, email: Isabel.chang@photonic-tech.com)

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