Ironwood
ELECTRONICS

Benefits of Signal Integrity (SI) Simulation for High Speed Socket and Adapter Design

Introduction

High-speed sockets and adapters continue to perform important functions for today's IC component and electronics packaging engineers. Whether for testing, prototyping, or production, these components typically require an ever-increasing level of electrical and mechanical performance. In the area of electrical performance it is particularly important that an accurate predictive model be available for performance at GHz frequencies. Rather than relying solely upon historical measures derived from complex test configurations, these predictive models as simulations are capable of providing accurate performance data in a timely as well as cost-effective manner. This data then serves as an aid to the design and test engineer relative to the initial selection of a proper interconnect design, and also serve as a predictor of performance over a variety of simulated end-use conditions. Since a beneficial simulation technique must be both reliable and versatile, the goal of this paper is to demonstrate this utility across a wide range of interconnect product designs.

Background

Over the past several years IC devices have continually increased in performance relative to both speed and functionality. These changes have been accompanied by new package styles featuring higher I/O counts with decreased spacing and reduced interconnect feature size. All of these factors combined create more demanding requirements upon the sockets and adapters used for interconnection.

At GHz level operating frequencies and beyond it has become increasingly important to understand the scattering and reflection properties of traveling waves when an interconnection network is inserted within a transmission line between an IC device and the attaching PC Board. S-parameter measurements in terms of reflection coefficients and transmission gain have typically been accomplished via the use of network and signal analyzers coupled with the use of special test fixtures and probing devices. Based on these measurements, network analysis provides the appropriate S-parameters from which impedance values may be derived and directly correlated via the use of Smith Charts.

Drawbacks to this traditional network analysis approach include the inability to probe within the center of an array for measurement data as well as the time and expense of performing such analysis. Computer-aided simulation offers an alternative approach to S-parameter derivation that is both timely and cost-effective. As a modeling technique, simulation also provides the capability to generate data across a complete array of

interconnection ports. A useful tool for this type of high-frequency simulation has proven to be the CST Microwave Studio™ offered by Computer Simulation Technology. The application of this technology to the simulation of high-speed interconnection sockets and adapters provide data that is accurate and reliable as well as adaptable to new designs of the future.

Comparison of Simulated and Experimental Results – GHz Socket

One type of high-speed socket interconnection media in use today utilizes conductive wires embedded within an elastomeric matrix (Figure 1). From a mechanical design perspective this matrix of conductors has proven to meet the mechanical requirements regarding tolerance variations from package to PC board while also providing the compression characteristics for repeated use over time. From an electrical performance perspective the modeling of this interface is shown in Figure 2 where the key parameters for modeling purposes become the conductivity, spacing, and length of the wire matrix along with the dielectric constant of the surrounding insulating material. Simulated insertion loss data from the modeling process is shown in Figure 3 for three different I/O locations. This may be compared to actual measured data in Figure 4 of a single I/O location. The 1dB loss point of the measured data occurs at approximately 10.5 GHz while the same loss point occurs in the simulated data at 10.7 GHz. This indicates a positive correlation of the measured data to the simulated data to within approximately 2%.

Figure 5 provides further data from the simulation process displaying both return and crosstalk results for several different I/O locations. Table 1 shows the translated appropriate inductance and capacitance results for these same data points.
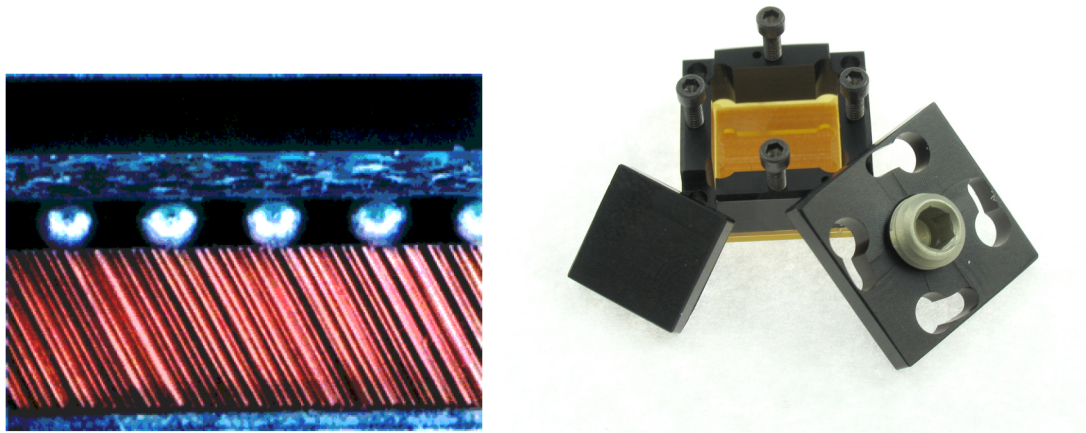
0.5mm GHz BGA socket simulation data

Figure 1 – BGA GHz socket with angled elastomeric interconnect
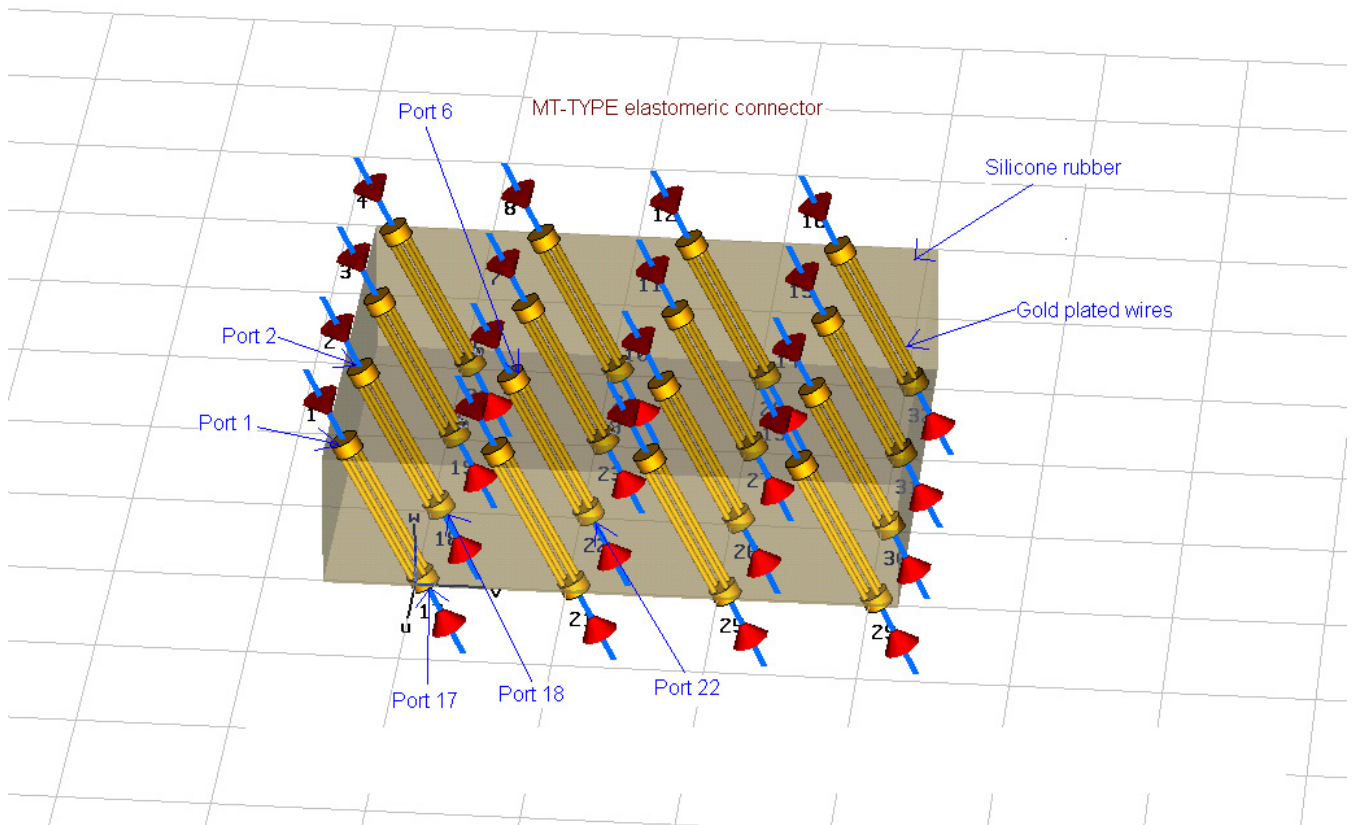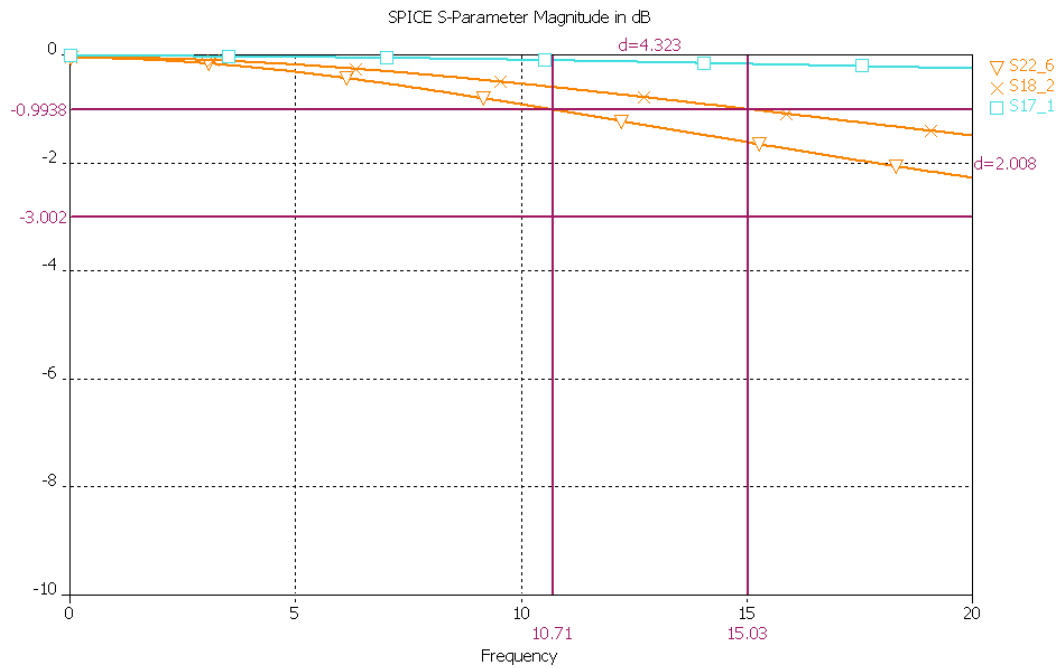
Figure 2: Elastomeric interconnect simulation based on 4x4, 0.5mm pitch BGA array

Figure 3: Simulated Insertion loss: -1dB at > 10 GHz (minimum bandwidth across the array).
Insertion loss of pin 1 is represented by S17_1, pin 2 is S18_2, pin 6 is S22_6.
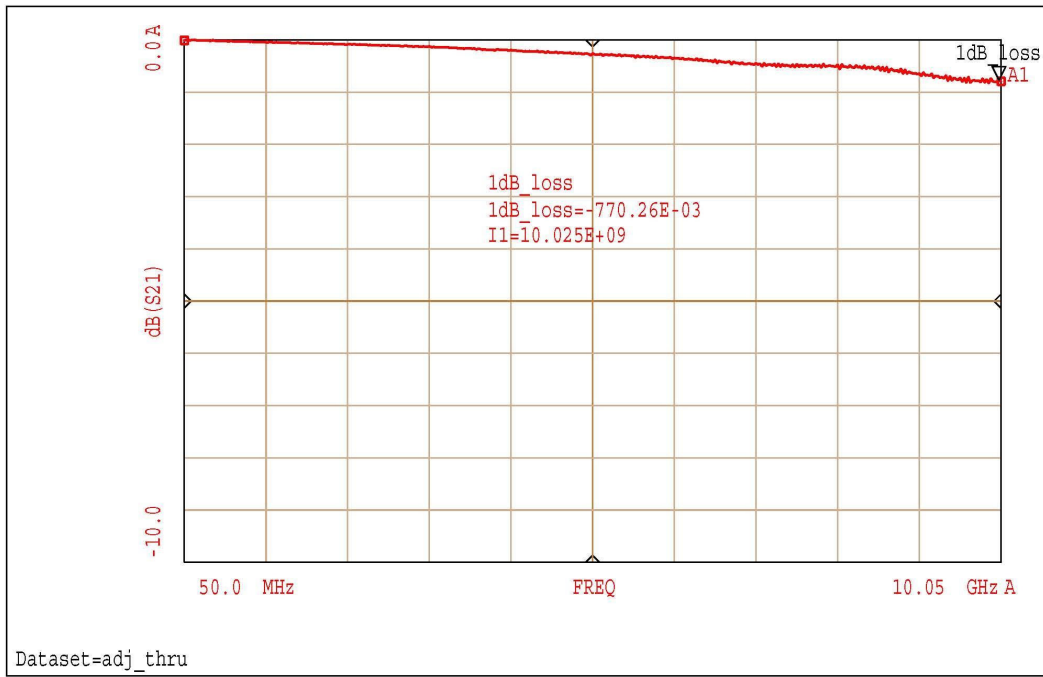
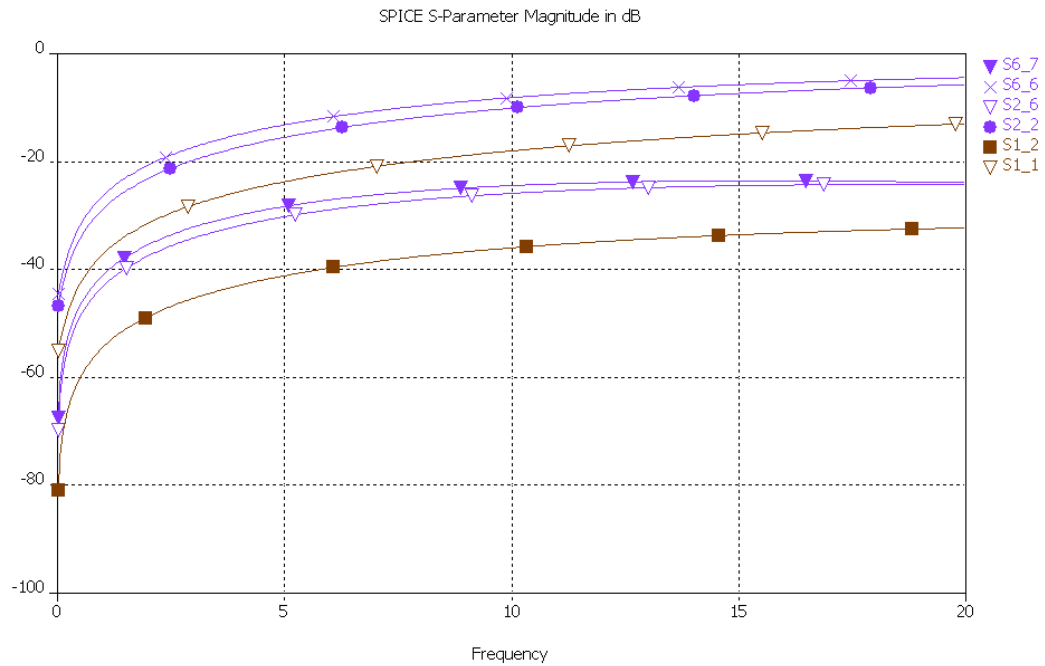**Figure 4: Measured Insertion loss: -1dB at >10 GHz.**

Figure 5: Simulated Return Loss and Crosstalk. S1_1 represents return loss at pin 1, S1_2 represents crosstalk between pin 1 and pin 2.

4

Capacitance (pF) to GND for all pins (1-16): 0.5mm GHz BGA socket

0.0090	0.0052	0.0052	0.0090
0.0052	0.0049	0.0049	0.0052
0.0052	0.0049	0.0049	0.0052
0.0090	0.0052	0.0052	0.0090

Self-inductance (nH) of the pins (1-16): 0.5mm GHz BGA socket

0.0359	0.0516	0.0516	0.0359
0.0516	0.0595	0.0595	0.0516
0.0516	0.0595	0.0595	0.0516
0.0359	0.0516	0.0516	0.0359

Mutual inductance (nH) for some pins: 0.5mm GHz BGA socket

Pin1	L_{12}=0.0031	L_{13}=0.00053	L_{14}=0.000036
L_{56}=0.0065	Pin6	L_{67}=0.01713	L_{68}=0.00172
L_{911}=0.00173	L_{1011}=0.01719	Pin11	L_{1112}=0.0065
L_{1316}=0.000037	L_{1416}=0.00055	L_{1516}=0.00307	Pin16

Table 1 - GHz BGA socket capacitance and inductance data

Simulation Versatility for Alternative Interconnect Designs

Simulation capability has also proven to be versatile to its application for a variety of interconnect designs. Figure 6 depicts the application of EM modeling to a more traditional pin and socket interface. Spaced on 0.8 mm, the conductive elements in this design consist of gold-plated contacts contained within an insulating material of traditional FR-4 PC board material. In this model the 1 dB insertion loss point (Figure 7) occurs at approximately 1.8 GHz revealing the useful range of this product for a variety of applications. Corresponding return loss and crosstalk (Figure 8), and electrical inductance and capacitance data (Table 2) are then provided. Additional simulation models have been developed for two additional designs. Figure 9 depicts a spring pin design with corresponding insertion loss shown in Figure 10, return loss and crosstalk shown in Figure 11. Figure 12 depicts an adapter for a QFN package with corresponding insertion loss data shown in Figure 13, return loss and crosstalk shown in Figure 14. More detailed results in terms of crosstalk, return loss, and impedance values are available for these designs as well.
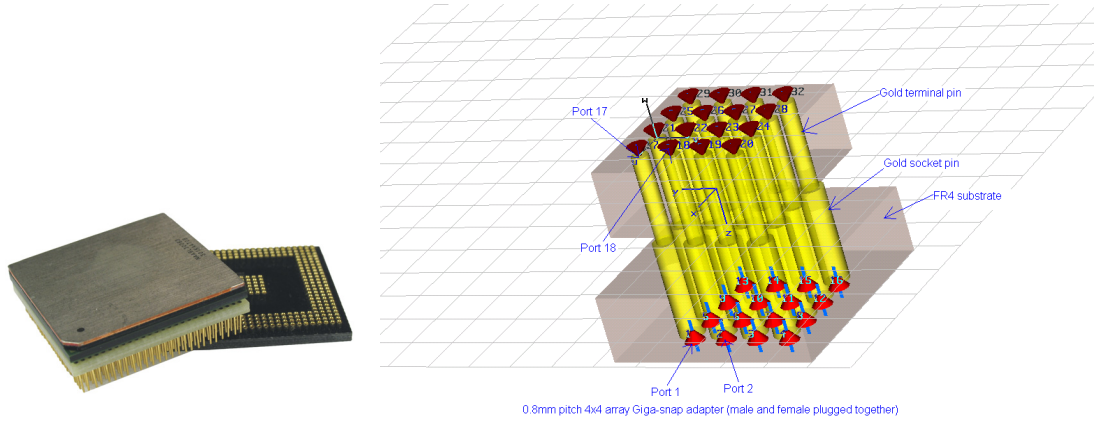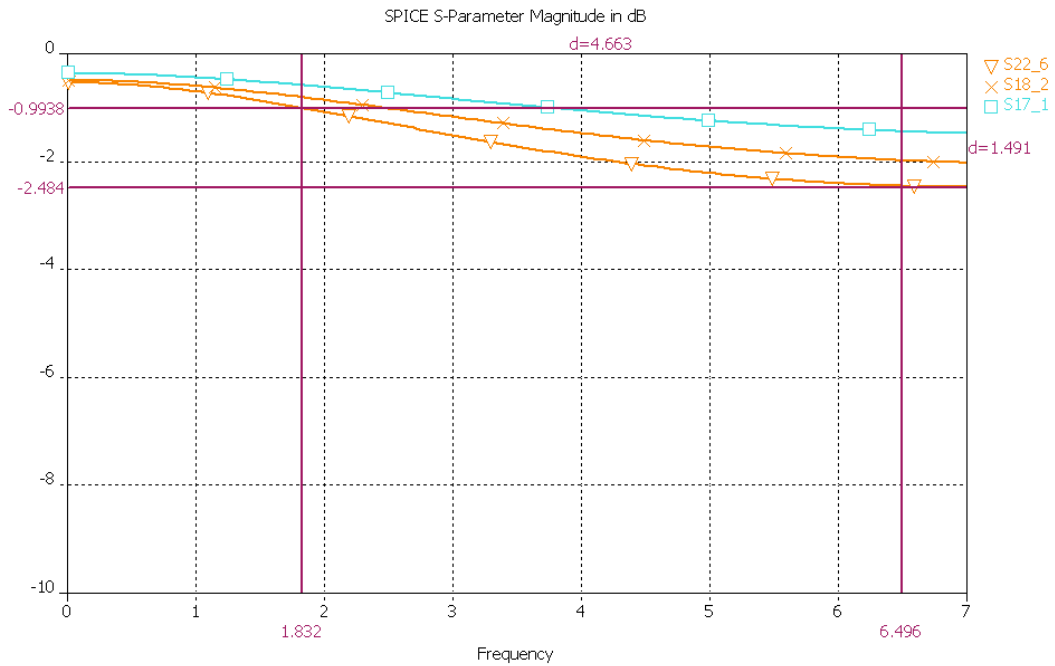
Giga-snaP™ adapter simulation data

Figure 6: Giga-snaP™ adapter model based on 4x4, 0.8mm pitch BGA array

Figure 7: Simulated Insertion loss: -1dB at > 1.8GHz (minimum bandwidth across the array)
Insertion loss of pin 1 is represented by S17_1, pin 2 is S18_2, pin 6 is S22_6.
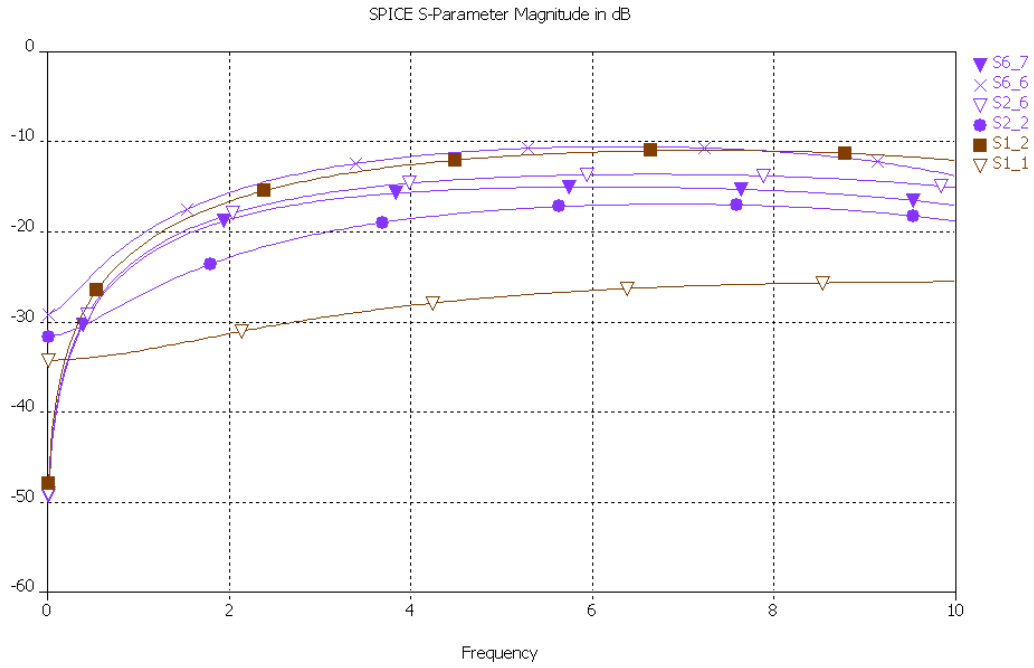
SPICE S-Parameter Magnitude in dB

Figure 8: Simulated Return Loss and Crosstalk. S1_1 represents return loss at pin 1, S1_2 represents crosstalk between pin 1 and pin 2.

Capacitance (pF) to GND for all pins (1-16): Giga-snaP™ adapter

0.2397	0.1080	0.1080	0.2397
0.1080	0.0054	0.0054	0.1080
0.1080	0.0054	0.0054	0.1080
0.2397	0.1080	0.1080	0.2397

Self-inductance (nH) of the pins (1-16): Giga-snaP™ adapter

1.5894	1.5798	1.5798	1.5894
1.5798	1.569	1.569	1.5798
1.5798	1.569	1.569	1.5798
1.5894	1.5798	1.5798	1.5894

Mutual inductance (nH) for some pins: Giga-snaP™ adapter

Pin1	$L_{12}=0.6412$	$L_{13}=0.3188$	$L_{14}=0.1666$
$L_{56}=0.6532$	Pin6	$L_{67}=0.6509$	$L_{68}=0.3455$
$L_{911}=0.3455$	$L_{1011}=0.6509$	Pin11	$L_{1112}=0.6532$
$L_{1316}=0.1665$	$L_{1416}=0.3188$	$L_{1516}=0.6412$	Pin16

Table 2 – Giga-snaP™ adapter capacitance and inductance data
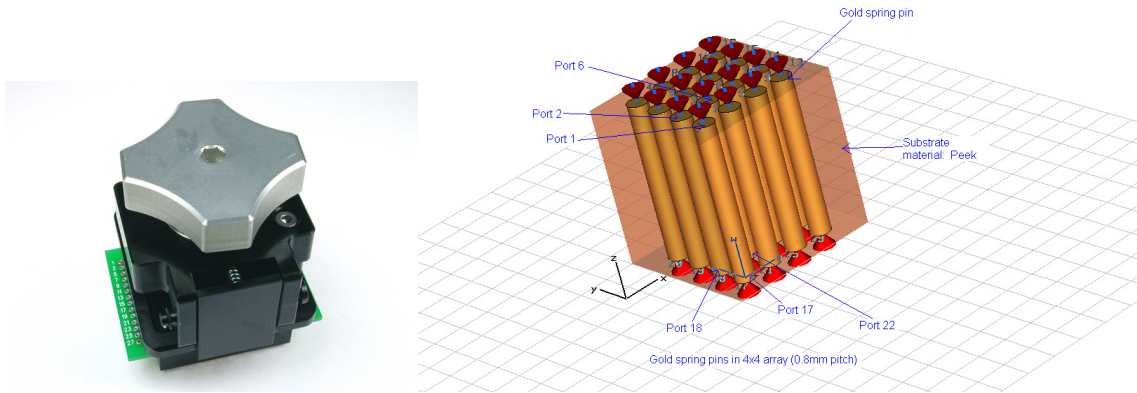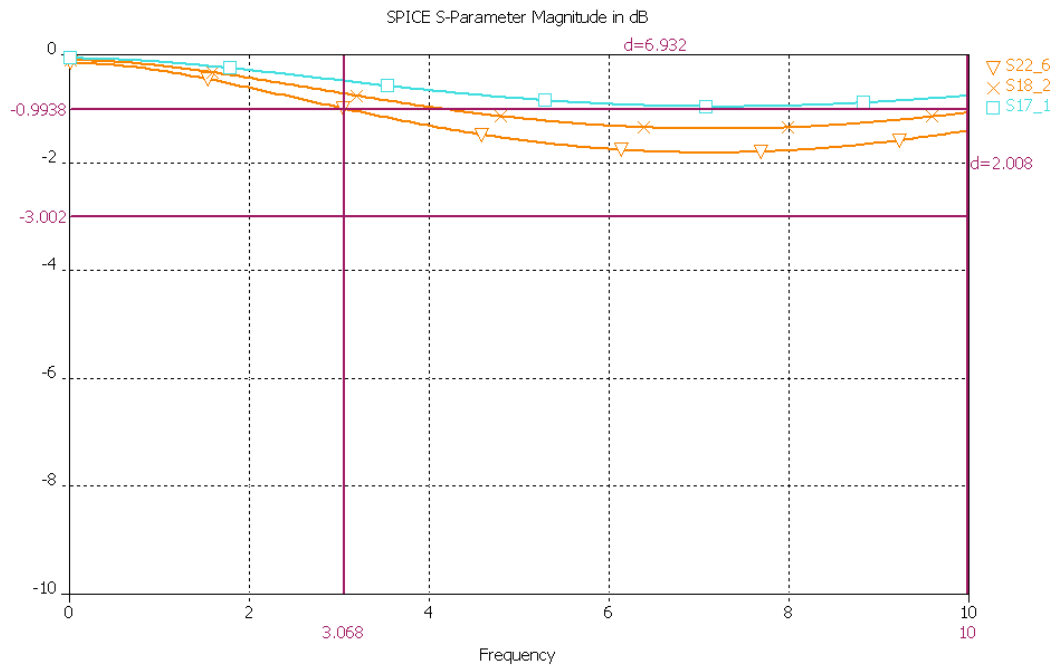
Spring Pin socket simulation data

Figure 9: Spring Pin model based on 4x4, 0.8mm pitch BGA array

Figure 10: Simulated Insertion loss: -1dB at > 3.0GHz (minimum bandwidth across the array)
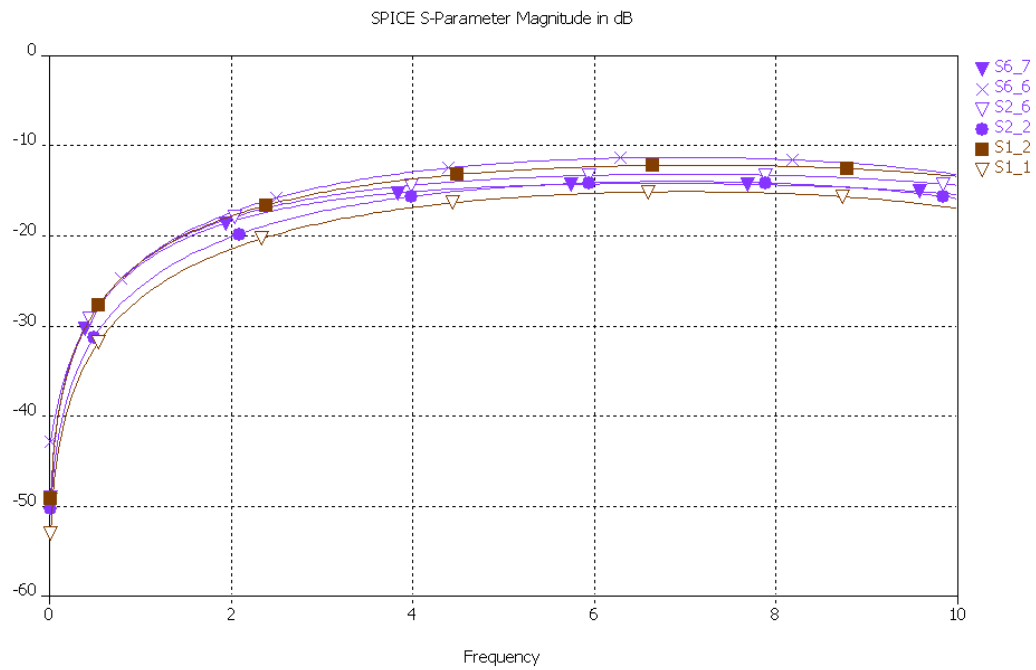**Insertion loss of pin 1 is represented by S17_1, pin 2 is S18_2, pin 6 is S22_6.**

SPICE S-Parameter Magnitude in dB

Figure 11: Simulated Return loss and Crosstalk. S1_1 represents return loss at pin 1, S1_2 represents crosstalk between pin 1 and pin 2.
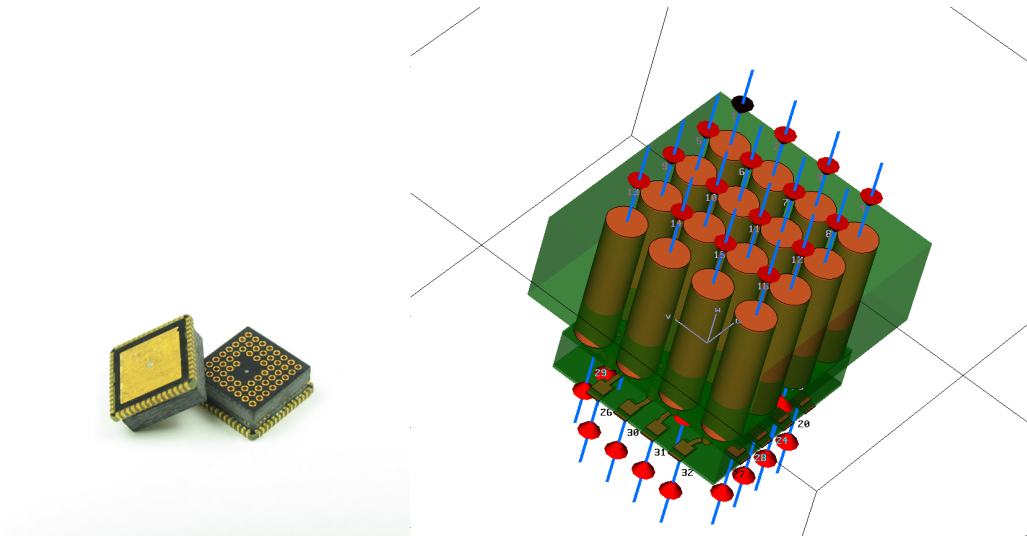
QFN Adapter simulation data

Figure 12: QFN adapter model based on 16 position to 4x4 array on 0.8mm pitch
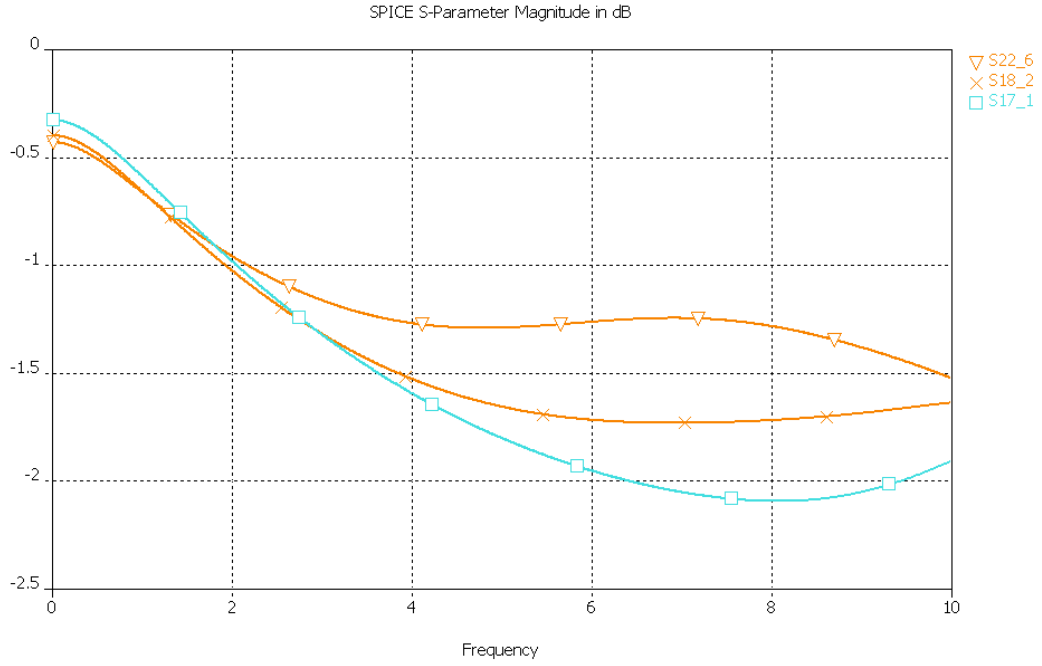
Figure 13: Simulated Insertion loss: -1dB at > 1.9 GHz (minimum bandwidth across the array) Insertion loss of pin 1 is represented by S17_1, pin 2 is S18_2, pin 6 is S22_6.
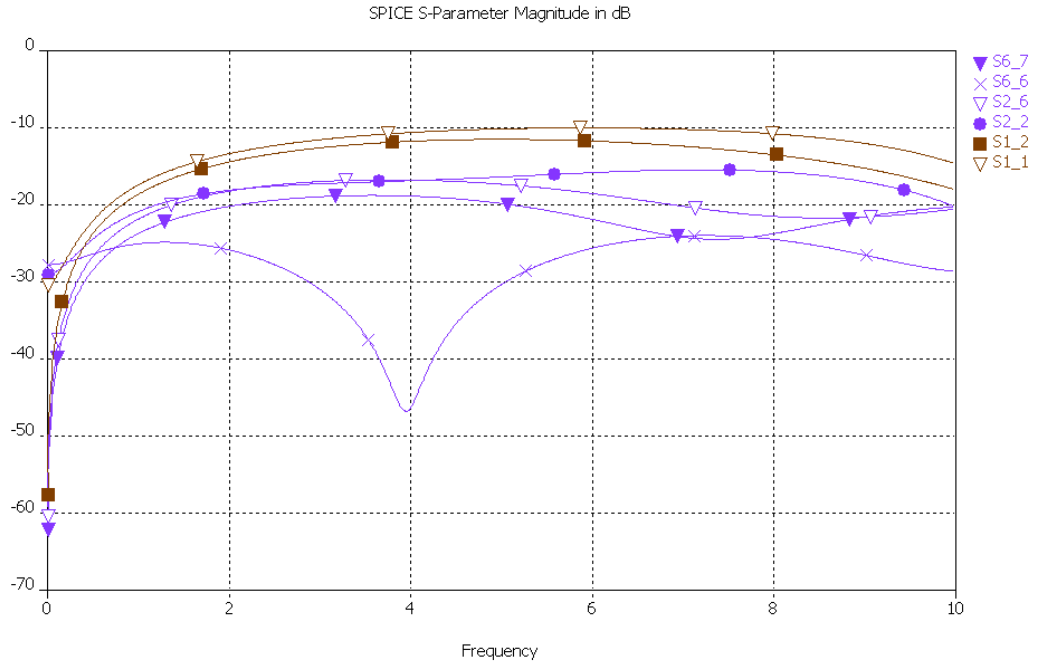

Figure 14: Simulated Return loss and Crosstalk. S1_1 represents return loss at pin 1, S1_2 represents crosstalk between pin 1 and pin 2.

Conclusion

Electromagnetic simulation modeling capability has proven to be an efficient and effective means for the interconnection provider to keep pace with the rapidly changing world of high-speed microelectronic device testing, prototyping, and end-product applications. The CST™ simulation package has successfully been applied to several different socket and adapter configurations. In so doing both the accuracy and versatility of this simulation technique has been demonstrated. When coupled with the timely and cost-effective manner in which similar models may be developed, the applicability of SI simulation as a useful tool for interconnection designs of the future may also be anticipated.

About Ironwood Electronics

Ironwood Electronics creates innovative VLSI interconnect solutions in prototype, test, and production applications for Design and Development engineers.

About CST

CST - Computer Simulation Technology develops and markets software tools for the simulation of electromagnetic fields in all frequency bands.

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