Review Light Sources for PIC and Si-Photonics

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2014-3-13

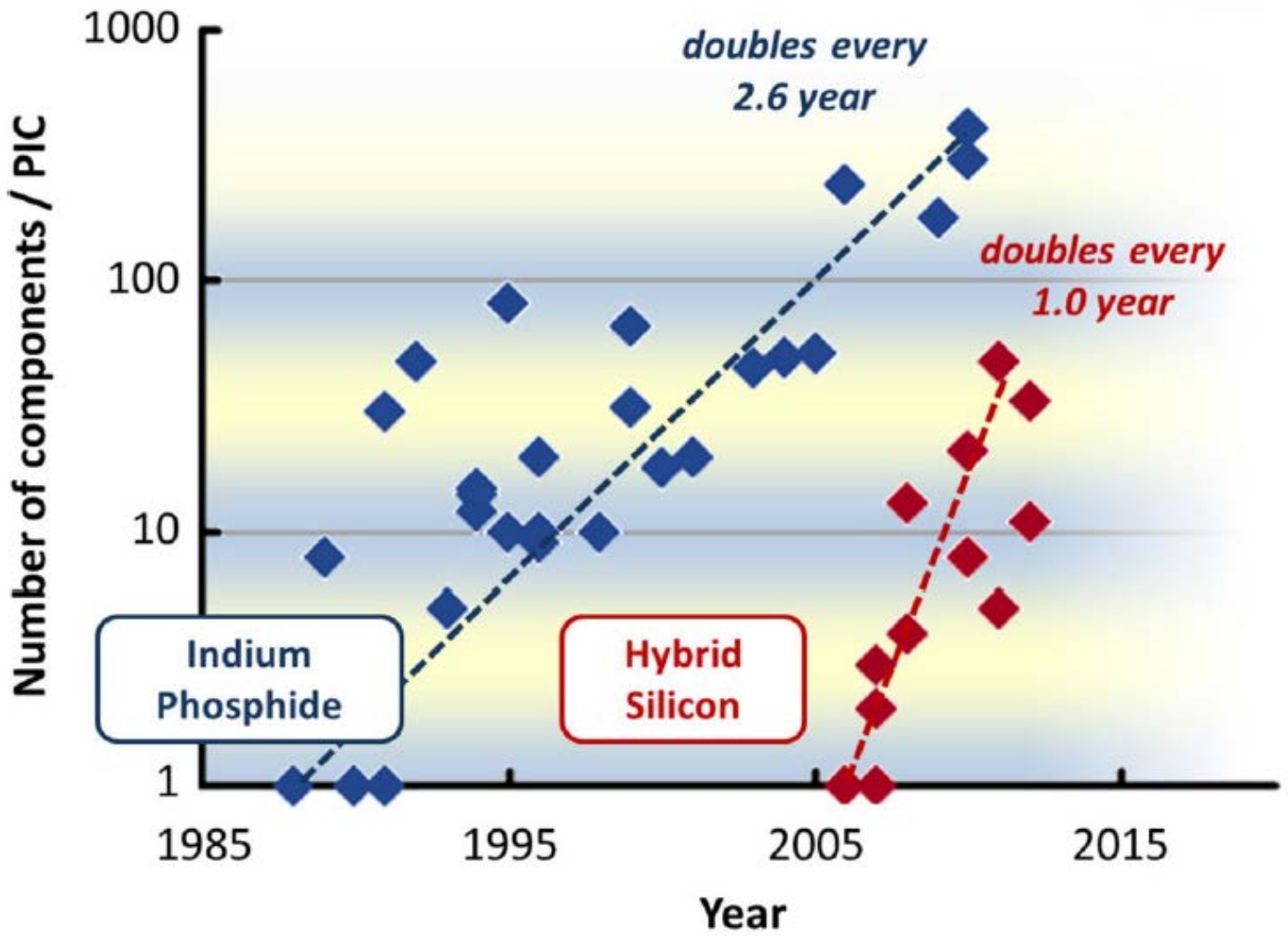
Motivation of PIC and Si Photonics Technologies

- Lower Cost
- Lower Power Consumption
- Smaller size, high density
- Device uniformity, higher yield
- Automated manufacturing
- Higher reliability and Long service life

Comparing InP PIC and Silicon Photonics

	InP base PIC	Silicon Photonics
Light source	Good light source material	Need InP light source
Process complexity and maturity	Less mature	Very mature
Scale, wafer size	Smaller size	Large scale

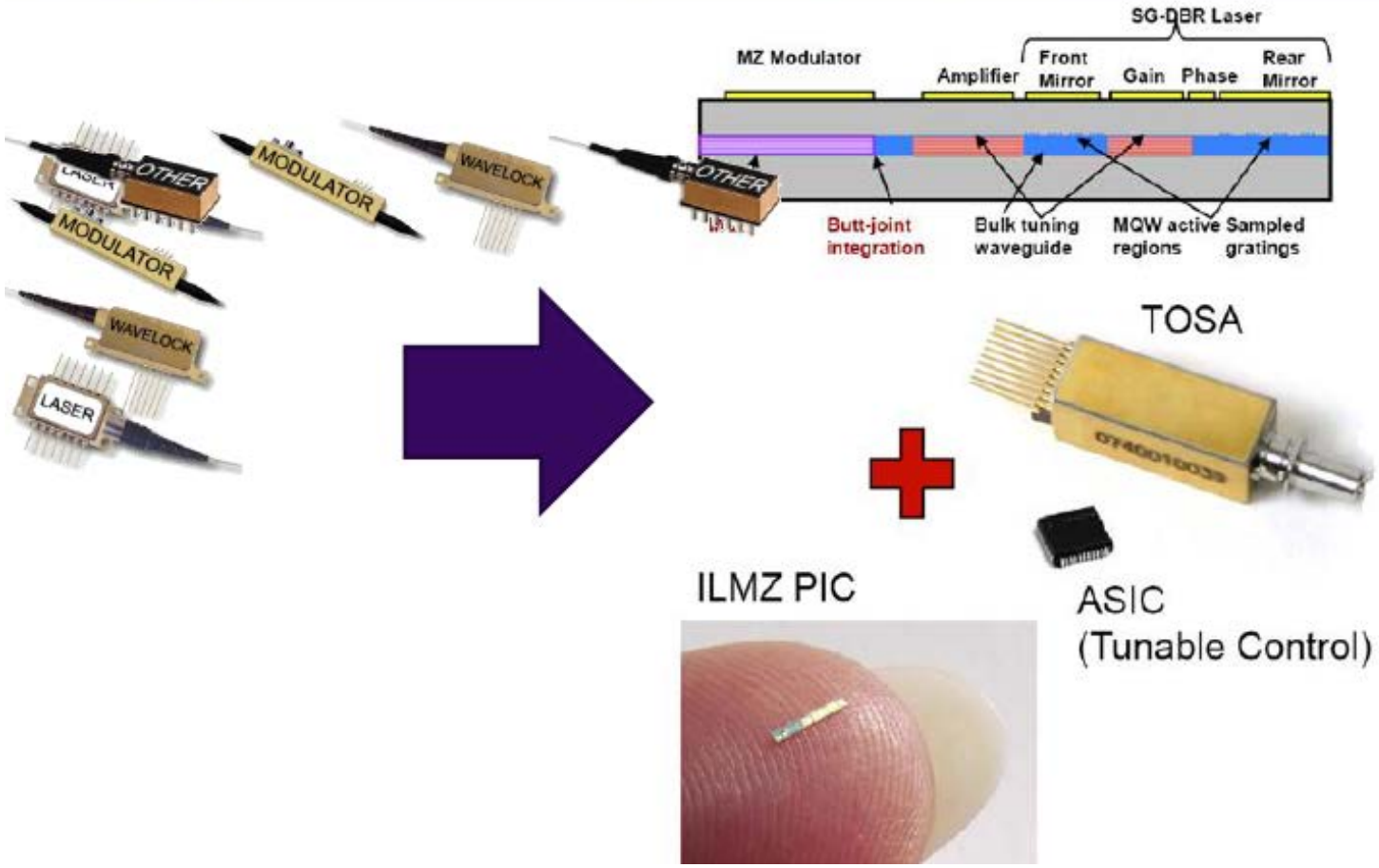
Summary of level of Integration in InP and Hybrid Silicon



Source: Martijn J. R. Heck (UCSB)

Example of InP based PIC

Small Scale PIC:
Integrated Laser Mach Zehnder (ILMZ)

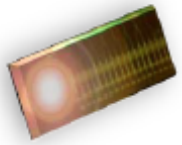


Source: JDSU

Example of InP based PIC

500G, Large Scale, Monolithic PIC Implementation

CAPACITY
RELIABILITY



500G
Tx PIC

500G
Rx PIC

COST
SIZE
POWER

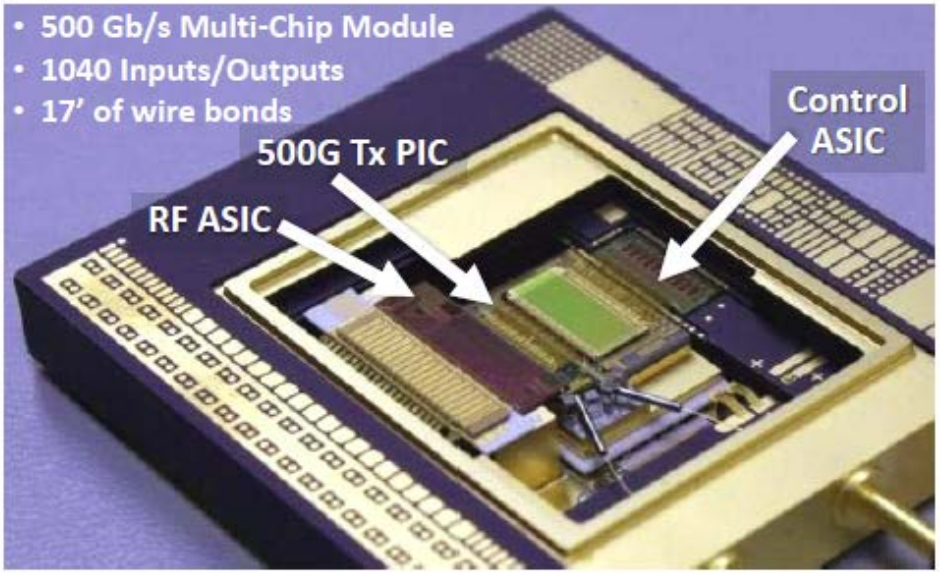
Number of channels	5 x 100G
Monolithic InP Chips	2
Optical elements	> 600
"Gold Box" Replacements	> 100
Fiber Replacements	> 400

Source: Infinera

Example of InP based PIC

500Gb/s Transmitter PIC

5 x 114Gb/s Transmitter
442 Elements: AWG mux, lasers, modulators, detectors, VOAs, control elements

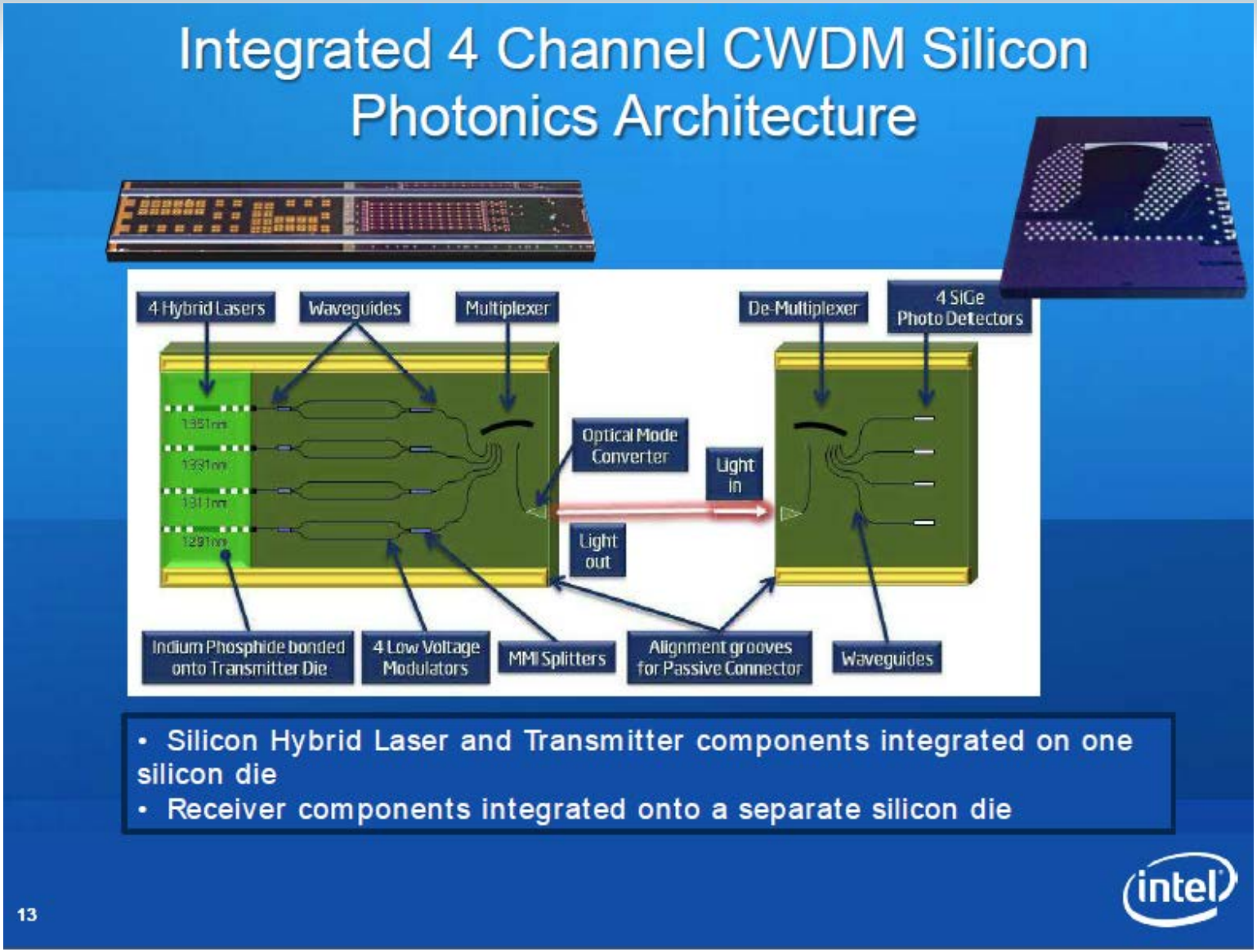


5 x 114Gb/s Tx PIC Module

infinera

Source: Infinera

Example of Si Photonics Architecture

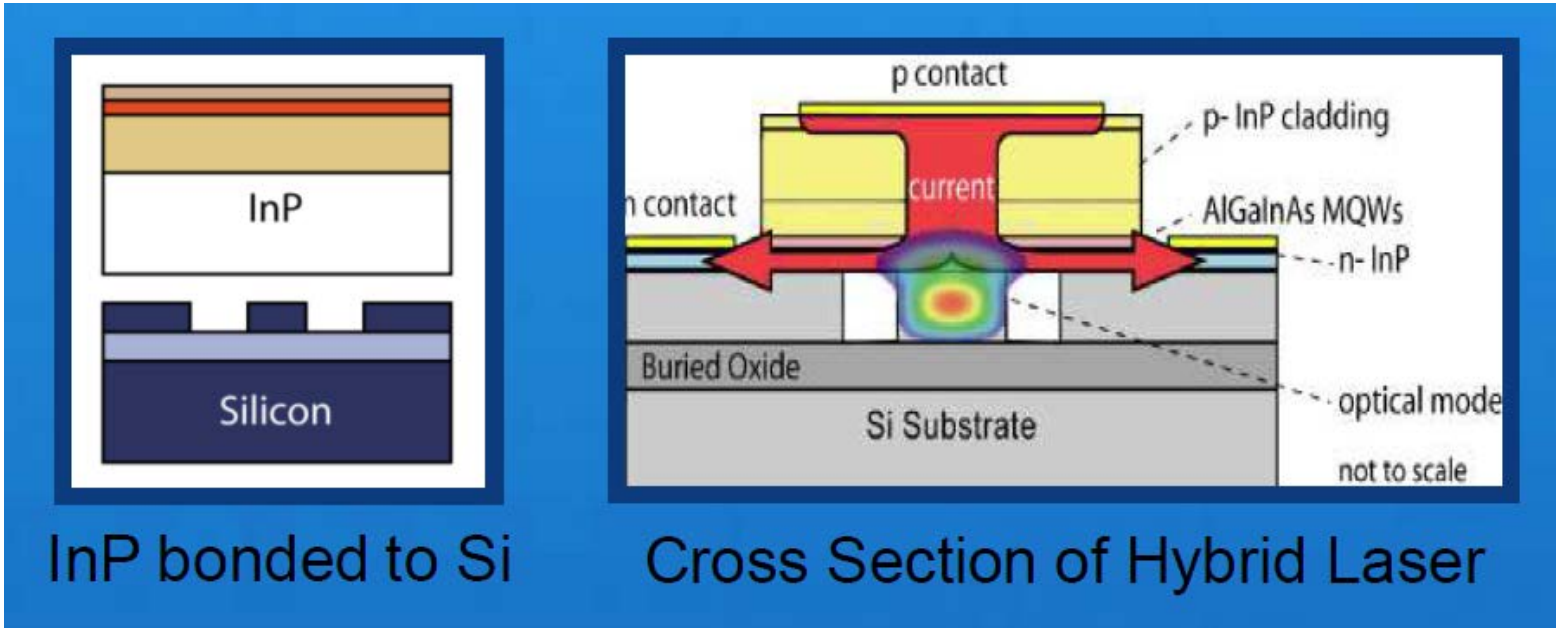


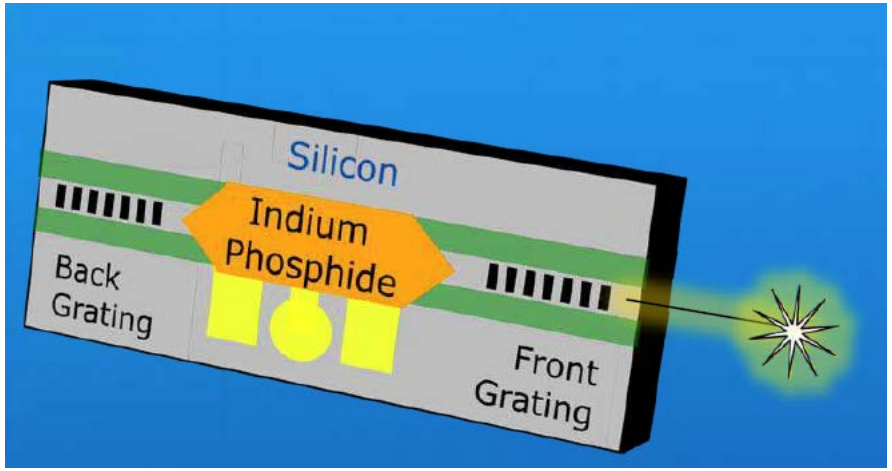
Source: Intel

Coupling light from InP Laser to Si chip is a challenge

- Butt coupling
- Bulk optics
- Grating coupling
- Due mode mis-match between InP laser and Silicon waveguide, Mode expander technology is needed

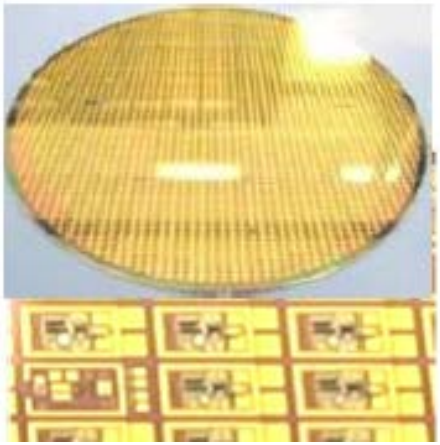
Example of light source for the Si Photonics





Source: Intel, UCSB

Example of light source for the Si Photonics



Source: Luxtera

New Technologies

New Device Technologies that enabling the PIC and Si Photonics Devices

Conventional vs. Etched Facet Technology

Conventional Cleaved Facet Process

1 Waveguide Formation
Contacts

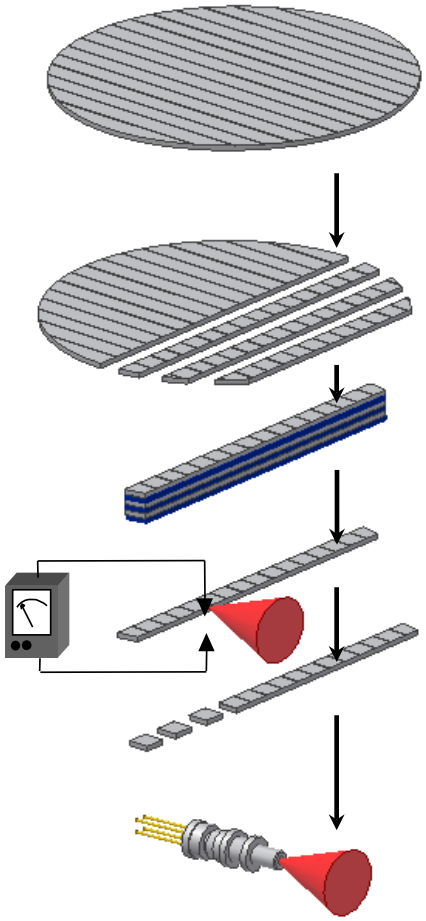
2 Cleave to Form Mirrors

3 Stack & Coat Mirrors

4 Test

5 Singulate

6 Package



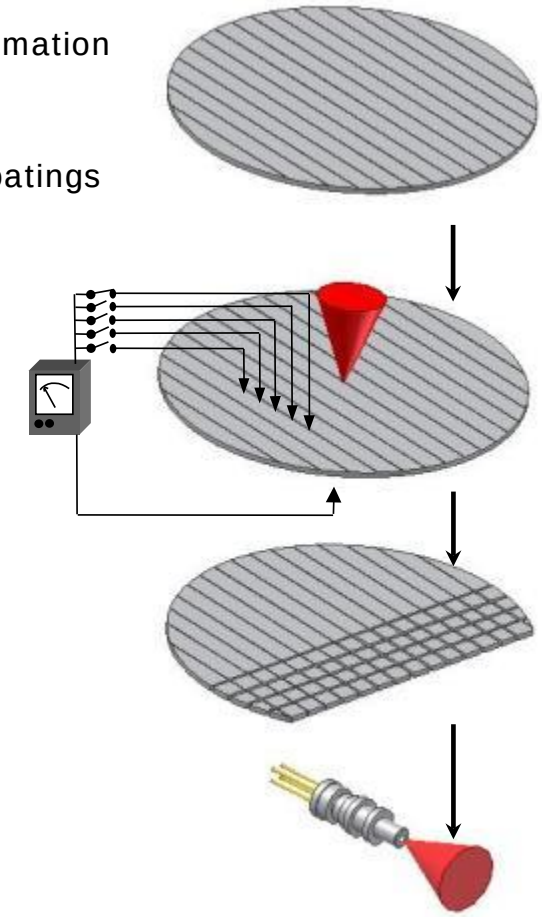
Etched Facet Technology Process

1 Waveguide Formation
Etch Mirrors
Contacts
Wafer Level Coatings

2 Test

3 Singulate

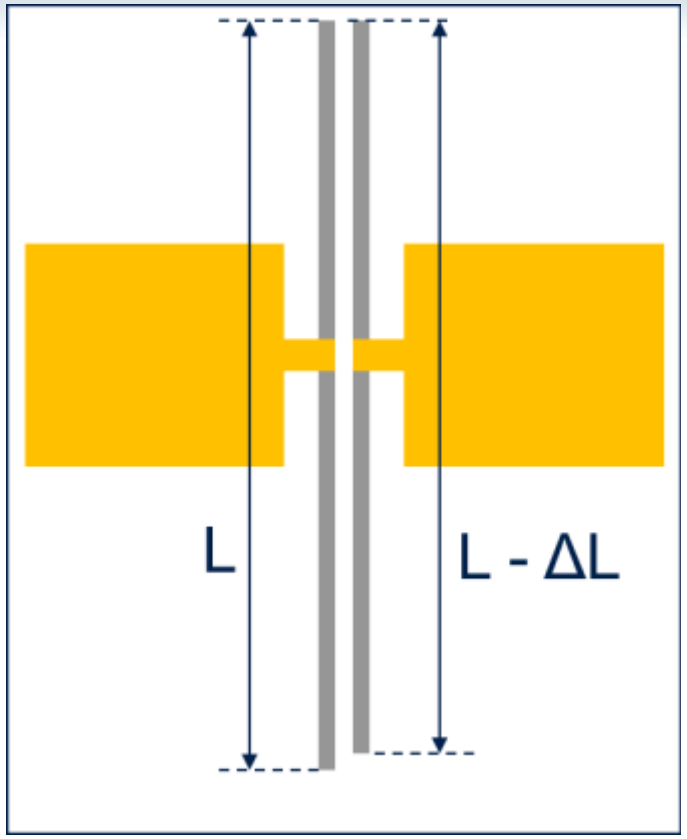
4 Package



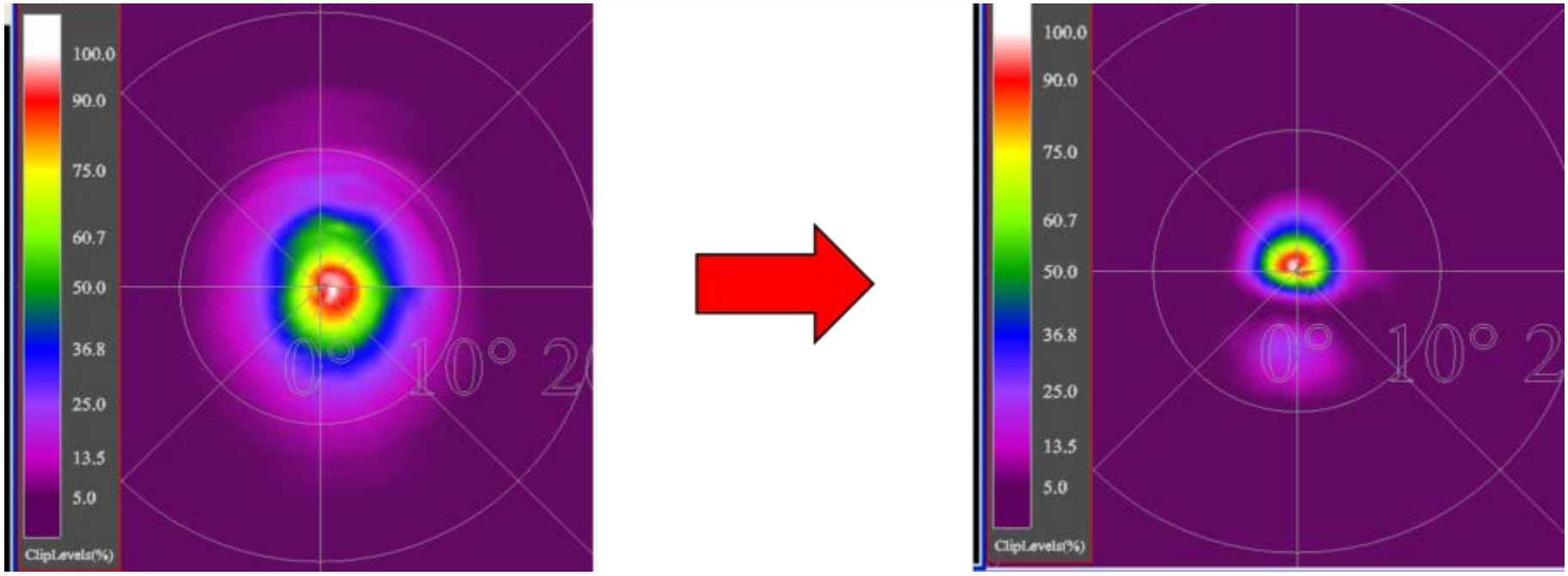
Over 50 million of laser sold using the EFT technology

Dual Laser Cavity

- EFT provides extremely precise control of dimensions and allows designers to put two laser cavities on one chip
- Designed so that one of two cavities operates with the correct phase
- Up to a doubling of chip yield for DFB lasers



Reduced Laser Beam Divergence



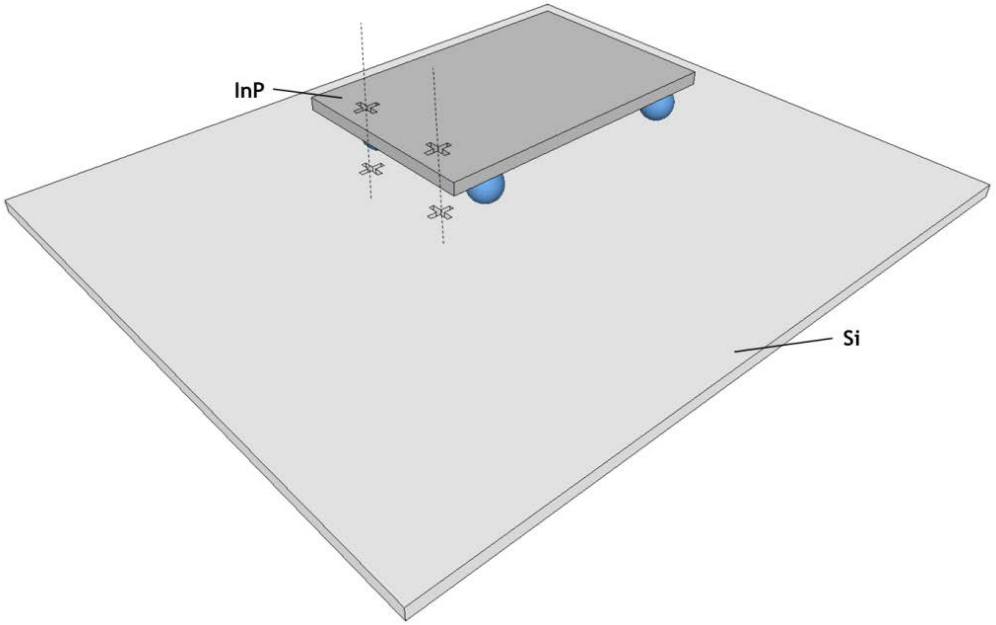
- **Reduced laser beam divergence to improve coupling to waveguide**
- **Reduce packaging cost and lower power consumption**
- **Need mode expander technologies (such as SAG, or EFT)**

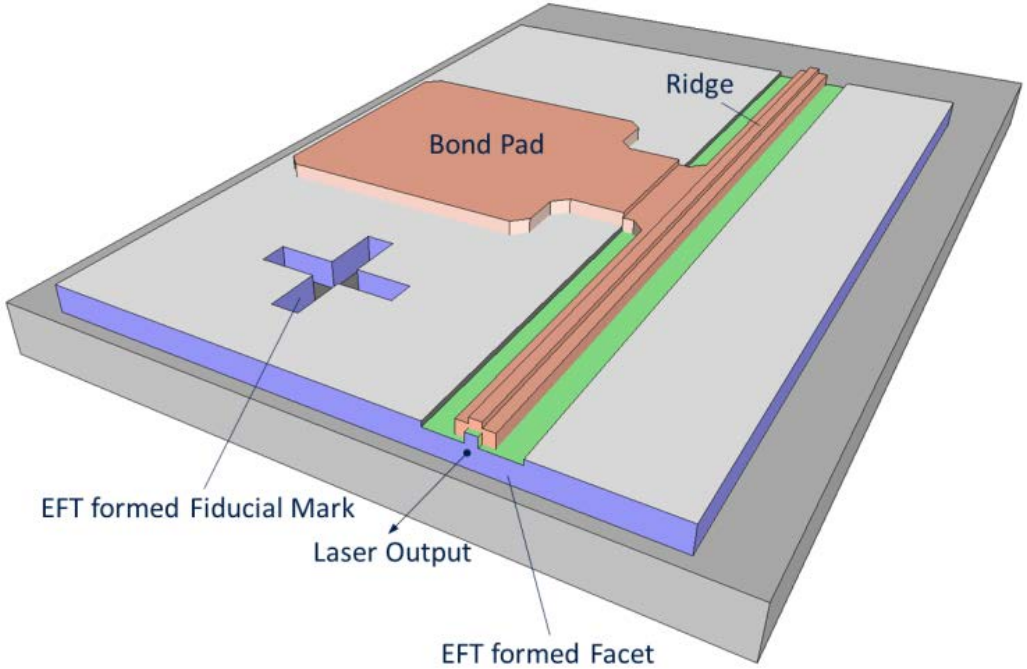
Deterministic Facet Placement

- **Place facets with extreme precision**
- **Eliminates the need to use costly active alignment; allows passive alignment**

Cleaved Facets	Etched Facets
Mechanical cleaving results in typical facet location ±5µm from desired location (at best ±2µm)	Facet locations determined by precision of lithography tools – Better than ±0.1µm
Requires active alignment to couple to other components	Can couple to other components with passive alignment

Deterministic Facet Placement



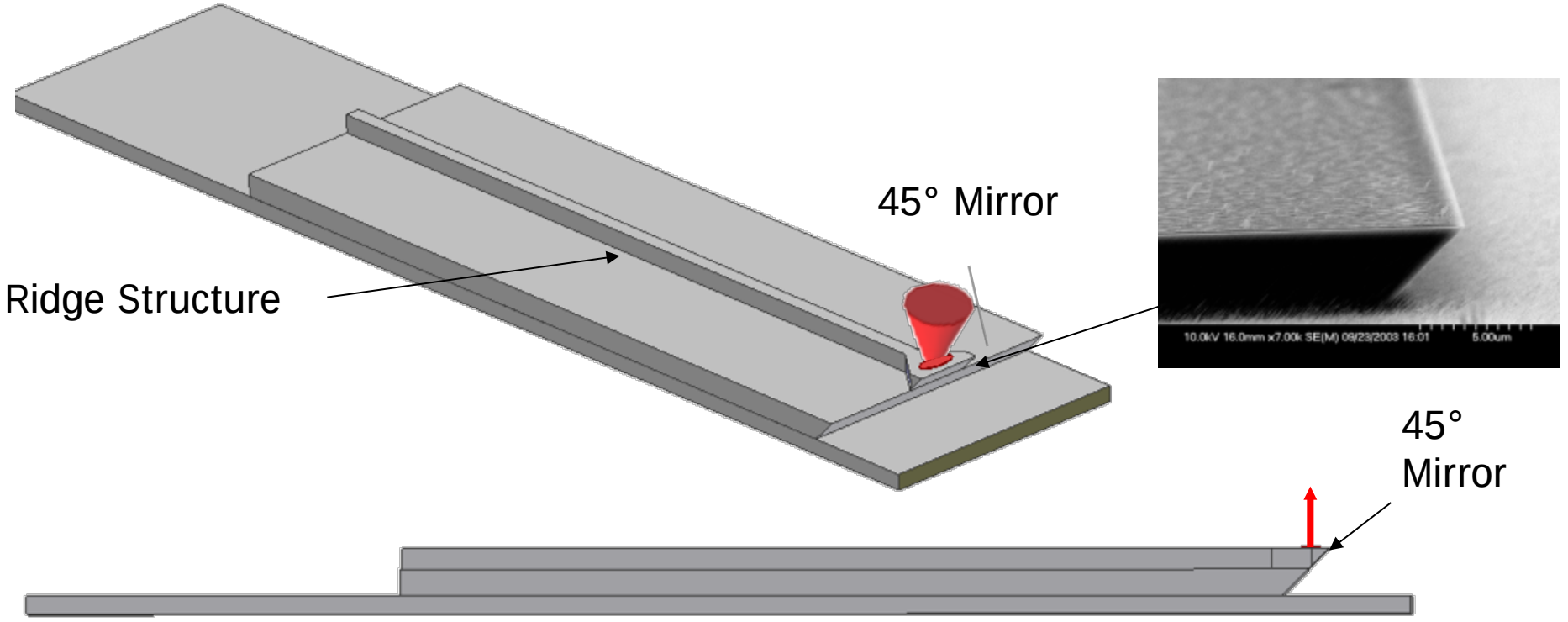


Passive alignment between InP source and silicon photonics chip through use of fuducials

Compatible with flip-chip bonding

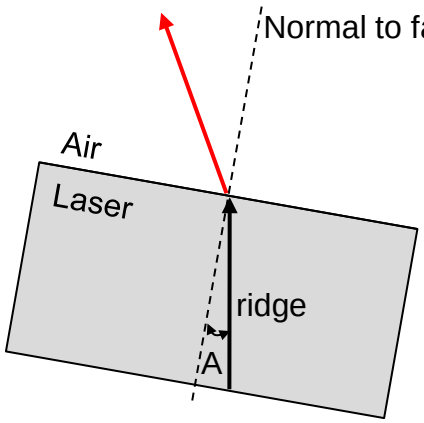
Angel Etching:
Horizontal Cavity Surface Emitting Laser ("HCSEL")

- **EFT allows etching independent of crystal orientation**
- **Smooth surface provides total internal reflection at angled facet; beam emitted perpendicular to laser cavity**
- **HCSELs take up less space than traditional vertical cavity lasers**

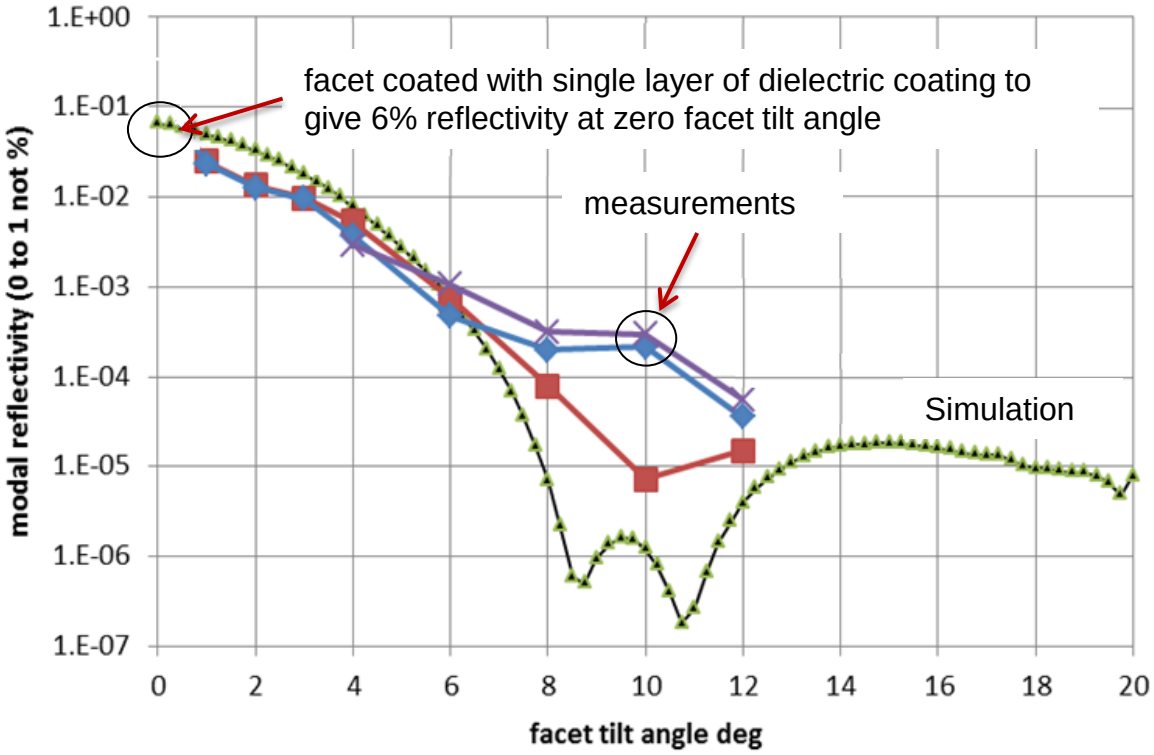


Low Reflectivity Facets

- Etched-facets allow low reflectivity values by using angled facets

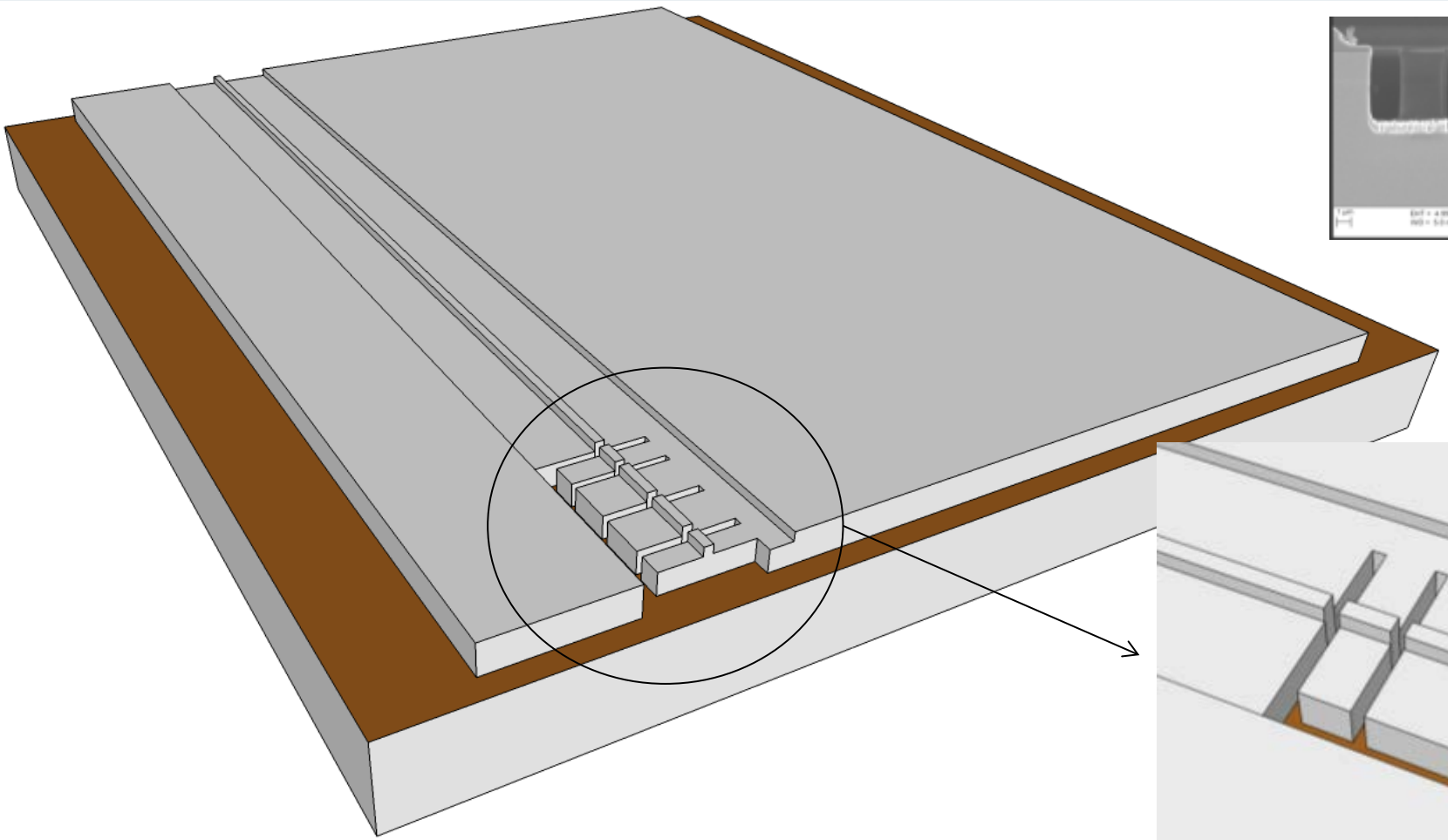


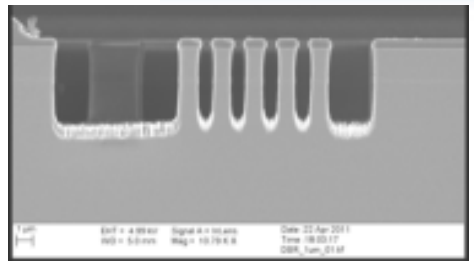
A = facet tilt angle

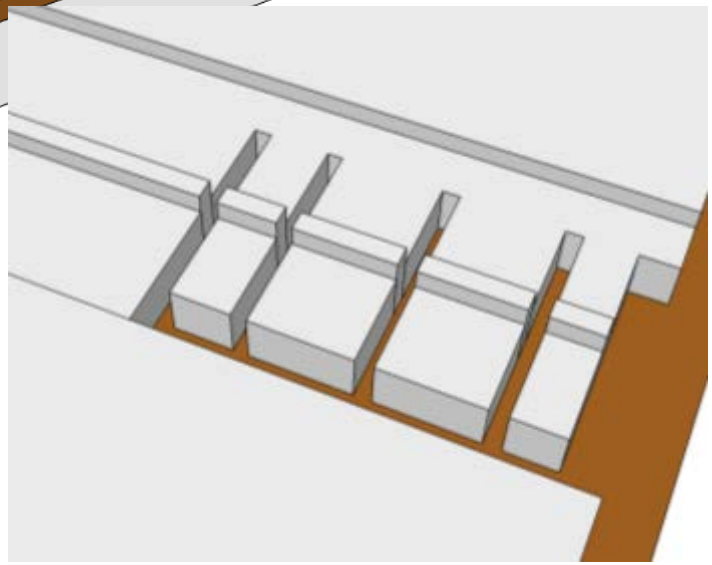


Low cost RSOA InP sources for silicon photonics

Single Longitudinal Mode (SLM) Laser with Etched Gratings

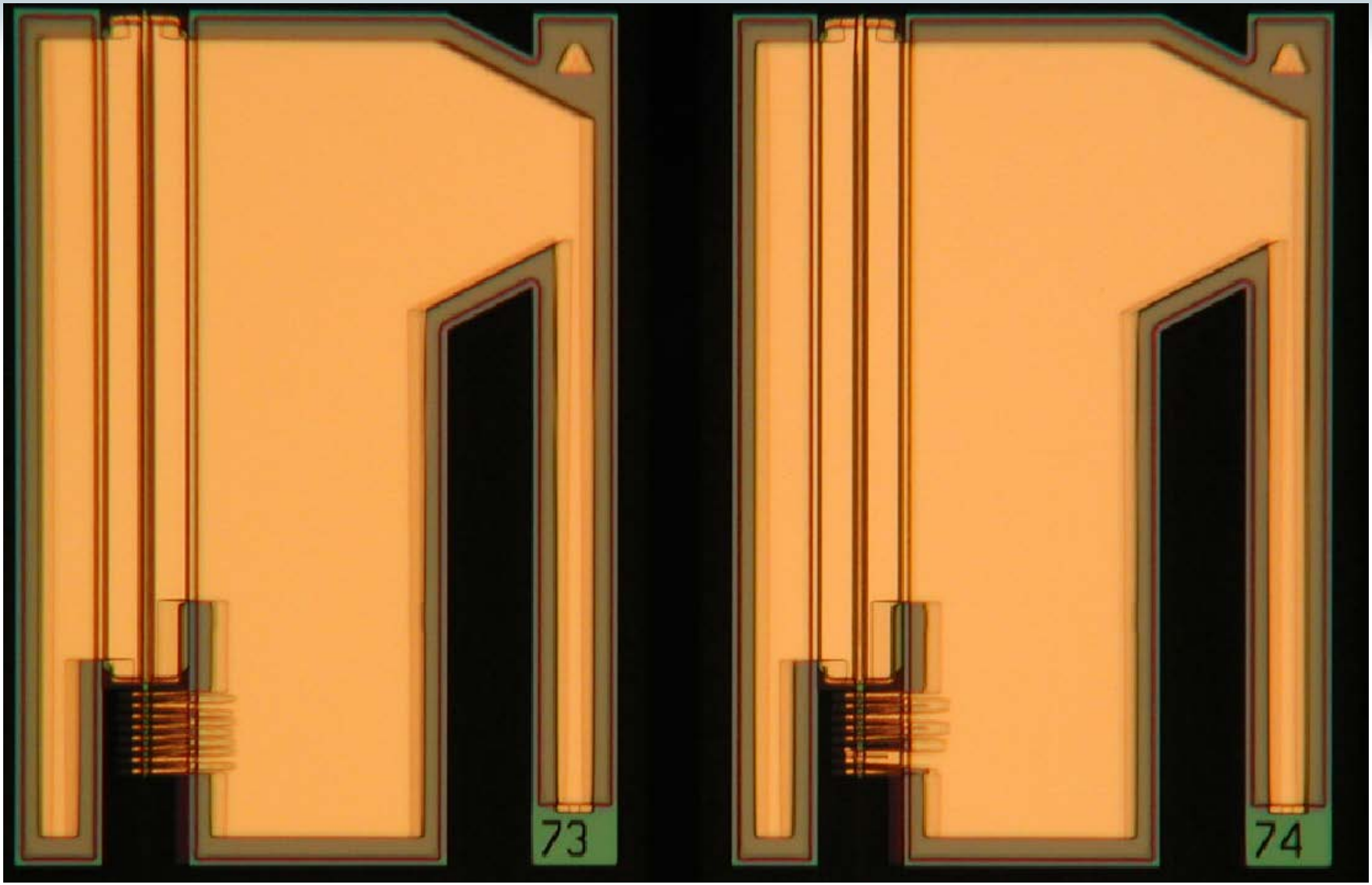




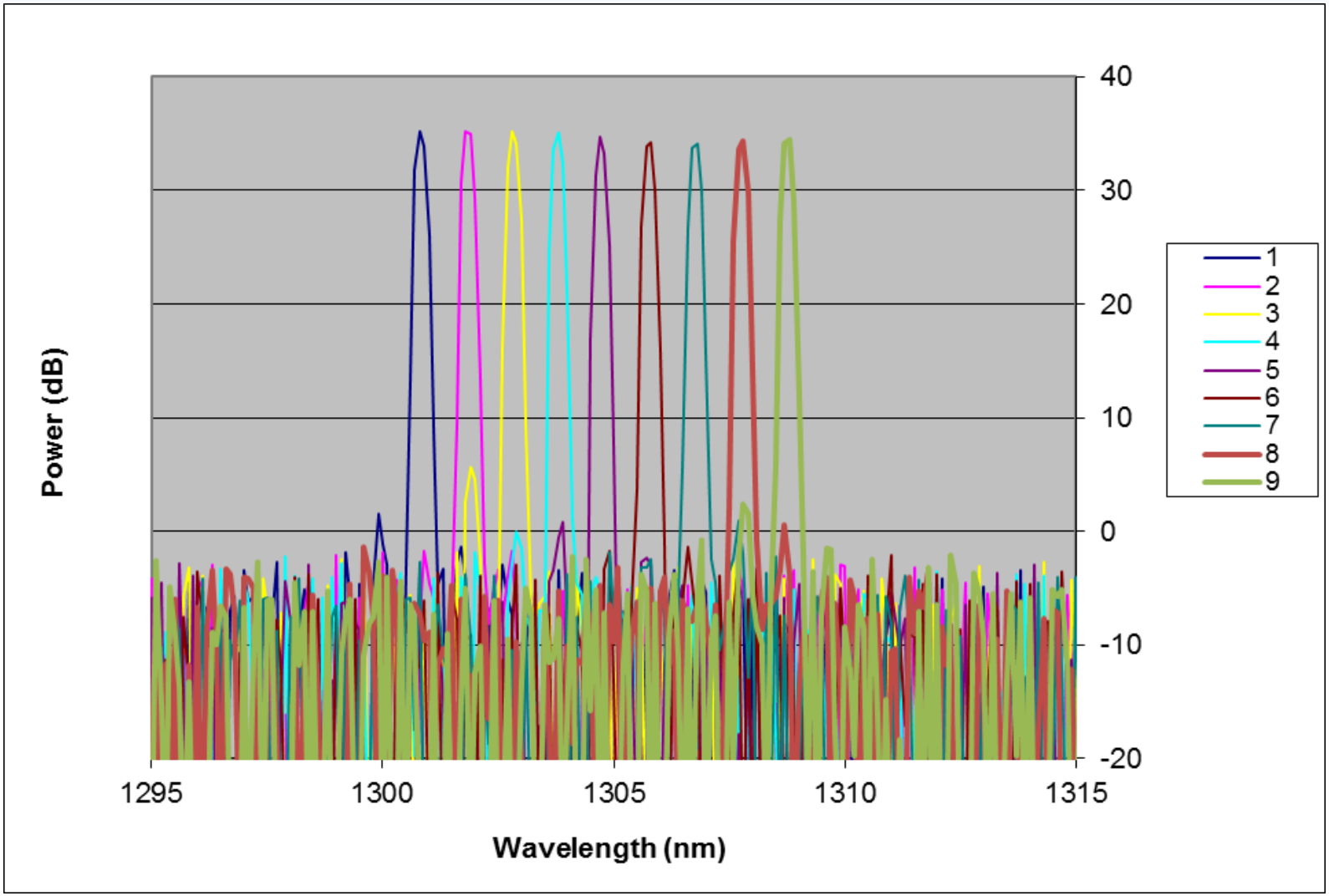


Gap in grating = multiple of half-wavelength of laser light

Example of an SLM Chip



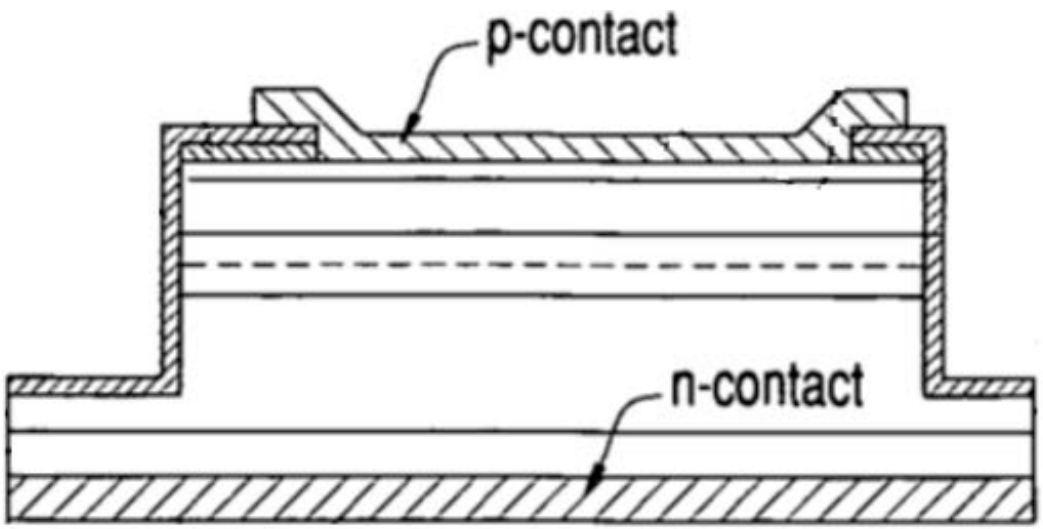
SLM Laser Array – 1nm Wavelength Spacing



Single mode 9 laser array with 1nm spacing

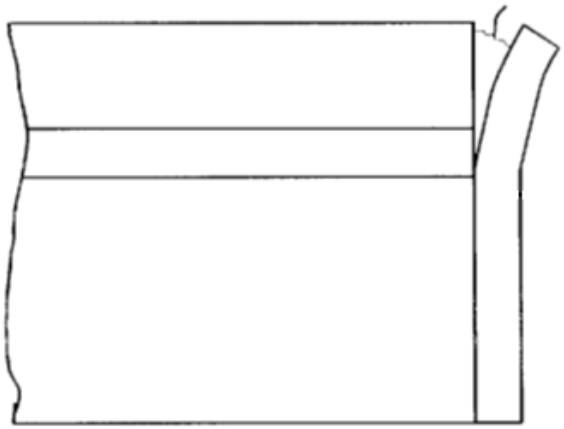
Operation in Non-Hermetic Environments

Etched Facet Laser



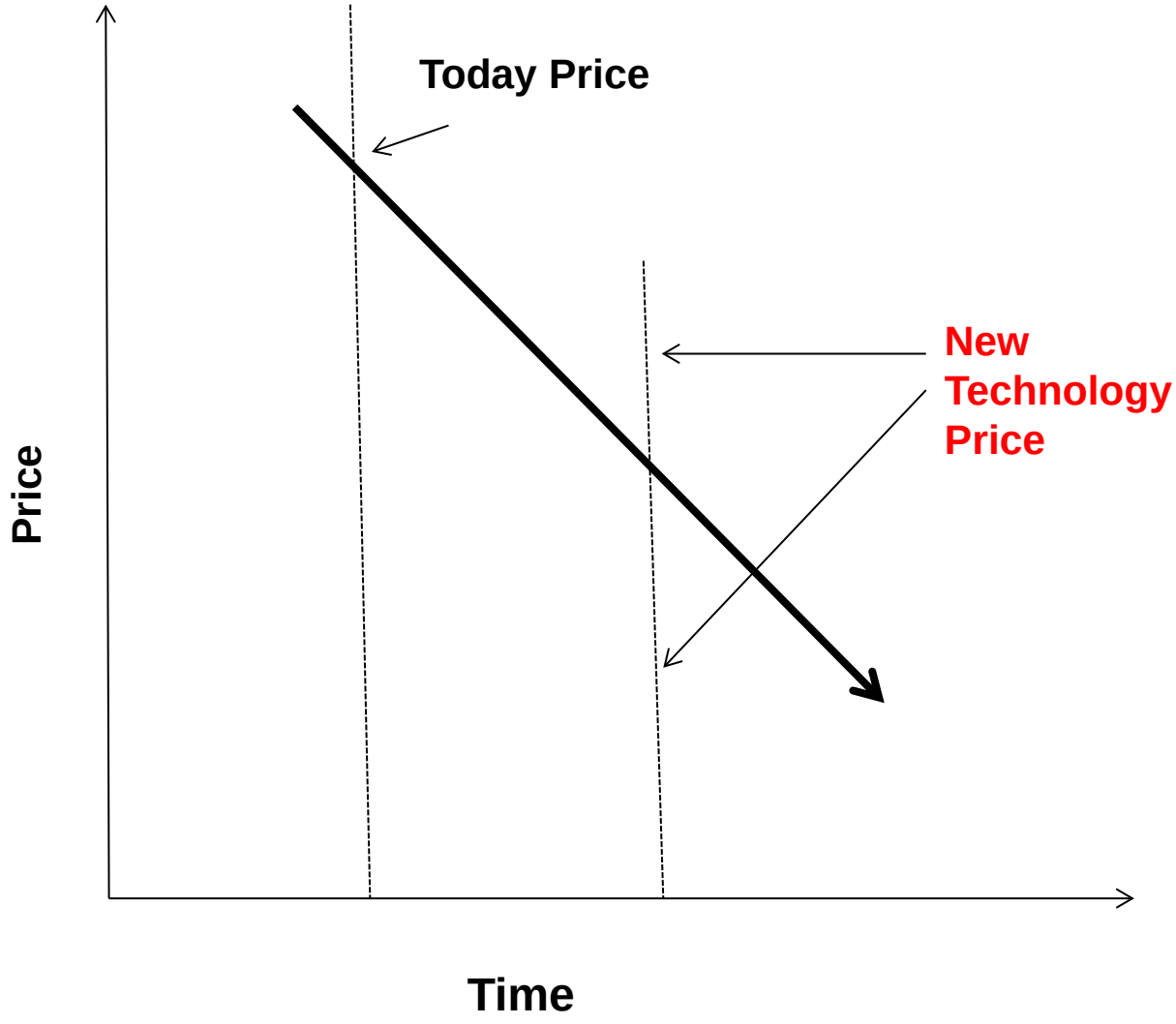
Cleaved Facet Laser

Possibility of delamination in non-hermetic environments



- Etched-facet lasers can operate in non-hermetic environments (direct exposure to temperature and humidity) since there are no exposed semiconductor surfaces to degrade
- Passivation on etched facet devices
  - Eliminates cost of bulky hermetic packages
  - Enables use in new applications

Price issue for new technology introduction



- Product price is dropping every year
- Need price incentive to design in (gain market share)
- Need volume to reduce cost
- Many fail examples in our industry (e.g. PON business)

New Challenge Ahead

- Can we find efficient ways to couple light to Silicon chips
- Can we improve the wall plug efficiency
- Can we improve the yield to demonstrate cost-effectiveness over the old technologies

Conclusion

PIC vs Si Photonics; Hype or Reality?

I believe both the InP base PIC and the Silicon Photonics technologies are real and they are happening

Each technology will find their places in theTelecom and Datacom Industries.

It depends on the applications