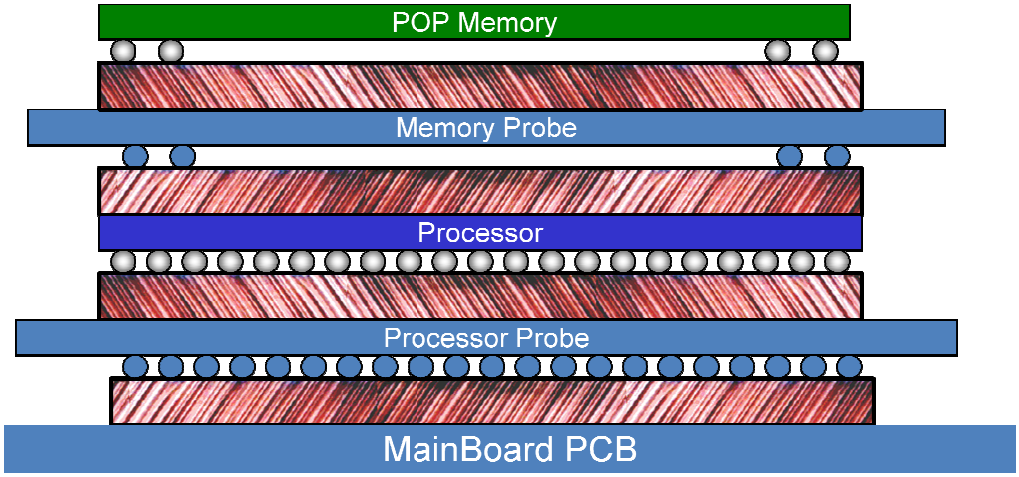
3D IC Development Needs Innovative Socket Solution

Ila Pal - Ironwood Electronics

Introduction

Evolution from cell phones with only a base-band processor and limited memory to today's high-end phones with an additional applications processor and memory has driven the industry to 3-D packaging solutions. 3-D packaging can be achieved via die stacking in one package, package-in-a-package stacking or package on package stacking. Each method has its pros and cons. Package on package stacking, which has been researched in a variety of formats**,** enables stacking of packages from different suppliers and mixed IC technologies. It also allows for burn-in and testing prior to stacking.



In a stacked package, typically the bottom package is processor and the top package is memory. Because of additional applications required by consumer industry, IC engineers add more features to their 2nd generation processor and the memory performance is increased by faster communication to the processor. Test engineers need a socket which can test 1st generation processor and memory. We have seen many product offerings for this one level stacked socket. In order to move from 1st generation to 2nd generation devices, a test engineer needs 2, 3, or 4 level stacked socket. During development, test engineer needs to use a processor probe in between processor and the main development board to connect with logic analyzer to perform the signal capability functions. Then test engineer uses memory probe in between the memory and processor to verify the performance of newer memory. The picture (Fig 1) below shows a typical four level interconnect enabling development sequence of 3D ICs. Designing a socket to accommodate these variations bring many challenges. In this article, two major challenges are addressed.

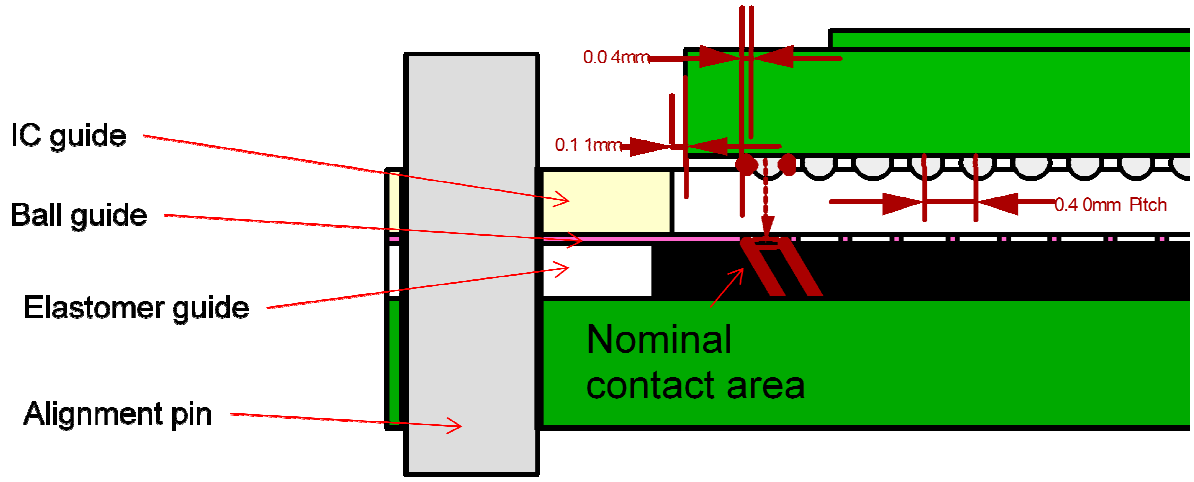
Force Challenges

The biggest of all challenge is force balancing. In a simple case, processor has 515 solder balls and the PoP (Package on Package) memory has 168 solder balls. Memory with 168 balls requires 5 lbs of force for optimum compression that results in less than 20 milliohms contact resistance per ball. Processor

with 515 balls requires 15lbs of force for optimum compression that results in less than 20 milliohms contact resistance per ball. In order to balance the force at each level, another 10 lbs of force is needed at the memory level. This will balance the force at processor level. When 15 lbs of force is applied to the memory with only 168 balls, the elastomer underneath memory will be over compressed. Also, there is potential of warping memory device due to high force. To counter balance, a sheet of rubber whose thickness can fill the gap between bottom side of memory device and top side of elastomer interface has been used. This rubber can absorb the extra 10 lbs of force resulting only recommended force on the elastomer section that was interfaced with memory device. Similar force balancing has to be accomplished at each level of interconnection if force variation exists.

Alignment Challenges

Similar to force balancing, alignment level challenges has been addressed at each interconnection level. Let us consider a simple case where a test engineer needs to test processor only. It is a simple one level interconnection. The following (Fig 2) picture shows typical variations in XY direction for a single stack up interconnect.



Elastomer is the “interconnect” used in this stack up. Top side of the elastomer interfaces with device ball and brings the electrical signal down to test board. Elastomer consists of gold plate brass wires embedded in silicone rubber. In order to have least resistance electrical path, greater than 50% of area with respect to pad/ball dimension to be made contact with top and bottom side. To ensure proper alignment, all the components are precisely positioned with one datum (alignment pin). The following scenario shows worst case situation.

PCB Alignment Hole position : +0.025mm

Ball guide Alignment Hole position : +0.025mm

PCB Pad location/Size : +0.05mm

=0.1mm off from nominal location

With 0.24mm minimum pad diameter for 0.4mm pitch BGA, elastomer contacts more than 58% of the pad with 0.1mm off from nominal location. This means pin alignment hole and ball alignment hole has to be manufactured with very tight tolerance ±0.025mm. This XY variation occurs on each level of the stack up. All the levels should ensure greater than 50% contact coverage area for the best electrical connection. Similar calculations have to be made for Z variations and manufacturing tolerances has to be updated such that >50% of pad is covered by elastomer. Alternatively, if spring pins are used instead of embedded wire elastomer for interconnect options; the alignment challenge is increased two fold. First, we have to add spring pin diameter tolerance. Second, we have to add the hole tolerance that positions the spring pin. In order to ensure proper electrical connection, manufacturing tolerances have to be very tightly controlled on these two additional factors which results in yield issues and high cost. Selecting appropriate interconnect medium plays major role in development cost.

Conclusion

New applications in communication industry are one of many demands help drive semiconductor industry towards 3D solutions. 3D packaging finds ever increasing usage in automotive, entertainment, medical, industrial, etc. 3D packages will be De Facto standard in future. Advancement in interconnect technologies are critical in enabling the IC system development process to move forward. Pitch, pin count and performance complexities increase in 3D packages due to consumer demand. Simple two level IC stacking requires four level interconnection for development needs. XYZ alignment challenges at each interconnect level push manufacturing capabilities to its extreme. Force balancing at each level requires innovative design and new materials with unique properties.

Author:

Mr. Ila Pal is VP of Marketing at Ironwood Electronics can be reached at ila@ironwoodelectronics.com